IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

Serial No.: 09/846,119

Filed: April 30, 2001

For: METHOD OF MAKING A PLANARIZED SEMICONDUCTOR STRUCTURE

§ Group Art Unit: 1763
§
§ Examiner: Goudreau, G.
§
§ Atty. Dkt. No.: 5298-04700
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§
§

CERTIFICATE OF MAILING
37 C.F.R. § 1.18

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

9-19-03
Date

Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, William W.C. Koutny, Jr., hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.

2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

CONCEPTION

3. As supported below, I, along with Yitzhak Gilboa, Steven Hedayati and Krishnaswamy Ramkumar, conceived of the subject matter claimed in the present application within the United States before June of 2000. The subject matter includes a method for forming a structure within a trench of a semiconductor topography.

4. Exhibit A attached hereto is a true copy of an invention disclosure form and attached pages which bear dates before June of 2000 corresponding to the conception of the invention. The actual dates for the first drawings, the first written description and first oral disclosure to others have been redacted.

5. Page 5 of Exhibit A describes the subject matter of the presently claimed case including the use of fixed abrasive polishing techniques to produce structures with a limited amount of dishing.

6. Exhibit B attached hereto is a true copy of a written description of the conceived subject matter, dated before June of 2000.

7. Page 2 of Exhibit B describes the subject matter of the rejected claims including the use of fixed abrasive polishing techniques to polish a layer deposited within a trench.

REDUCTION TO PRACTICE AND DILIGENCE

8. From at least a time just prior to June of 2000 through the filing of the application on April 30, 2001, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to June of 2000 through the filing of the application on April 30, 2001.

9. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to June of 2000 through the filing of the application on April 30, 2001.

10. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

William W.C. Koutny, Jr.

Date: 7/10/03

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S) DISCLOSURE NO PM00028

***

A. Name [illegible] CY Initials [illegible] Empl. No. [illegible] Ext. No. [illegible]

Citizenship U.S.A. Dept # [illegible] Home Phone No. [illegible]

Home Mailing Address [illegible]

***

B. Name William Bintoro CY Initials B/S Empl. No 135 Ext. No. 2653

Citizenship [illegible] Dept # [illegible] Home Phone No. [illegible]

Home Mailing Address 2555 Homestead #45 Santa Clara, CA 95051

2555 Homestead 45 95051

***

C. Name Steven Hedyati CY Initials SH Empl. No. 8534 Ext. No. 4556

Citizenship US Dept # 3103 Home Phone No. 408-927-9187

Home Mailing Address 424 Valley Quail Circle San Jose CA 95120

2. TITLE OF INVENTION Method of making Shallow trench isolation Structure

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings Redacted
Where can first drawing be found Redacted

B. Date of first written description Redacted
Where is description found Redacted

C. Date of first oral disclosure to others Redacted
To whom? Discussed with KTR, SH, BK

4. CONSTRUCTION OF DEVICE

A. Date Completed
B. Was prototype made?
C. By whom made?
D. Where can the prototype be found?

Inventor's: [signature] Date 1/21/00

Inventor's: [signature] Date 5/24/00

Inventor's: [signature] Date 5/24/00

Witnessed, Read, and Understood by: [signature] Date 5/24/00

Witnessed, Read, and Understood by: [signature] Date 5/24/00

(Each page upon which information is entered should be signed and witnessed.)

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S) DISCLOSURE NO _____

***

A. Name Ramkumar CY Initials KTR Empl. No. 3305 Ext. No. 2726

Citizenship INDIAN Dept # 3108 Home Phone No. (408) 255-1031

Home Mailing Address 1193 LYNBROOK WAY, SAN JOSE, CA 95129

***

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____

Citizenship _____ Dept # _____ Home Phone No. _____

Home Mailing Address _____

***

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____

Citizenship _____ Dept # _____ Home Phone No. _____

Home Mailing Address _____

2. TITLE OF INVENTION _____

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings _____
Where can first drawing be found _____

B. Date of first written description _____
Where is description found _____

C. Date of first oral disclosure to others _____
To whom? _____

4. CONSTRUCTION OF DEVICE

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C. By whom made? _____
D. Where can the prototype be found? _____

Inventor(s) _____ Date _____

Inventor(s) _____ Date _____

Inventor(s) _____ Date _____

Witnessed, Read and Understood by: _____ Date _____

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Exhibit A- page 2

CYPRESS SEMICONDUCTOR

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5. **TEST OF DEVICE**

A. Date: _____ Witness(es): _____

B. Results: _____

6. **SALE**

A. Was invention sold or offered for sale? Yes___ No✓
B. Was invention used to make, assemble or test a commercial product? Yes___ No✓
C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes___ No✓
D. Actual or estimated date of first sale, offer or commercial use _____
E. Is invention part of a product for which there is a data sheet? Yes___ No✓ (If yes, attach a copy)
F. Actual or estimated date of publication, release or availability of data sheet _____

7. **USE**

*** A. Is invention presently being used? Yes_____ No✓

*** B. In what product or process is invention presently being used?

_____

Are there specific plans for its use in near future? In what products or processes?

RAM-8

8. **RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS**

5,972,792 / 4010573 and 5782675 / 5919282
4393629 / [illegible]

9. **WAS INVENTION** Conceived (Yes____ (No✓ Constructed (Yes____ (No✓ Tested (Yes____ (No✓ during performance of Government Contract?

Contract Number _____
(Give Full Contract Number)

==========

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventor(s): [signature] Date [illegible]
Inventor(s): [signature] Date [illegible]
Inventor(s): [signature] Date [illegible]
Witnessed, Read, and Understood by: [signature] Date [illegible]
Witnessed, Read, and Understood by: [signature] Date [illegible]
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Exhibit A - page 3

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
2. Describe old technology, if any, for performing the function of the invention. Provide references, if available.
3. Indicate the disadvantages of the old technology.
4. Describe your invention and its construction, showing the changes, additions and improvements over the old method.
5. Give details of its operation (i.e., how is your invention used?), if not already described under 4.
6. State the advantages of your invention over what has been done before.
7. Indicate any alternate component(s) and/or method(s) of construction.
8. If a joint invention, indicate what contribution was made by each inventor.
9. Describe the features that are believed to be new.
10. State opinion of relative value of invention.

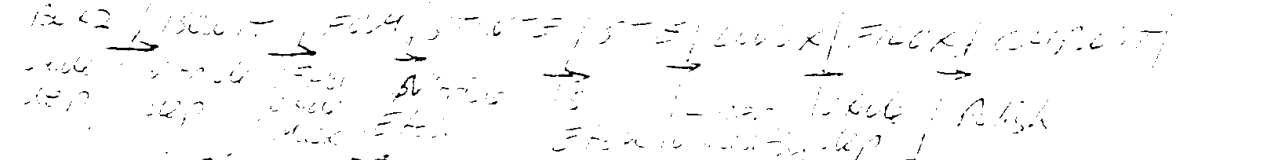
***

11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

==========

1. The purpose of the invention is to improve the manufacturability of STI and reduce cost, this is done by reducing processing steps

2. Current technology (AT-no TDX) calls for the following steps:



Inventor(s): _____ Date: 8/24/05

Inventor(s): _____ Date: 8/24/05

Inventor(s): _____ Date: 8/24/05

Witnessed, Read, and Understood by: _____ Date: 8/24/05

Witnessed, Read, and Understood by: _____ Date: 8/24/05

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Exhibit A - page 4

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

(3.) Disadvantages addressed by invention:

1. Thick nitride - layer required to overcome poor selectivity in Stacy etch
2. Process this means can induce stress defects
3. Additional etch required to etch nitride
3. Oxide step after trench etch which can result in step stringer
4. Thicker oxide fill deposition to overcome step induced by nitride.

(4) The current invention has three options for using Fluorine plasma as the ~~primary~~ method of polish. The main advantage of fluorine plasma is the negligible amount of residue compared to current slurry process. The second advantage is self planarizing so no more reliance on fill

Option I – No Nitride Hard mask

In this option, a thick pad oxide film is grown on base oxide. Trench etch completed. Once step is done, the wafers are cleaned. After trench etch oxide fill is done in the trench and cover the entire thickness of the trench depth including step. Oxide fill is done the same as for Stacy. Using Fluorine plasma is a reduced pressure or a-sacrificial. The key ~~is~~ is [illegible] to [illegible]

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Witnessed, Read and Understood by: _____ Date _____

Witnessed, Read and Understood by: _____ Date _____

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Exhibit A - page 5

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

Option II - Deposit Thin Nitride -

grow base oxide grow thin layer of Nitride (0-500 Å) expose field oxide mask, Etch nitride, Deposit fill oxide polish down to ~~nitride~~ stop on oxide at a predetermined Residual oxide above the nitride. Strip remaining oxide. Strip remaining nitride.

Option III

grow base oxide deposit nitride, expose field Etch trench, Deposit fill oxide, polish to nitride/pad layer use wet strip to remove remaining nitride, use dry/wet strip to remove oxide, Due to use of Etch Rate differences of Deposited to wet etched oxide, this option Possible w/ minimal strip of nitride/oxide. Note: (C) - Easy adjustment of width properties of thin oxide/nitride allowing the use of less or no nitride layer (D) - Elimination of nitride strip, Etch, Deposition process to thick layer to planarize step.

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 6

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

(8) equal resistance

(9) Fixed abrasive polish, no polish stop, different polish step

(10) - Invention will enable reduction of cost of ownership compared to Step.
- enable STI polish without requirement of hard mask.
- enable STI polish with reduced step height budget required for 193 nm lithography.

Inventor(s) _____ Date _____

Inventor(s) _____ Date _____

Inventor(s) _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

(Each page upon which information is entered should be signed and witnessed.)

Option 1

- No Nitride HM
- Stop after flatness - fixed abrasive
- Wet dip to below Si

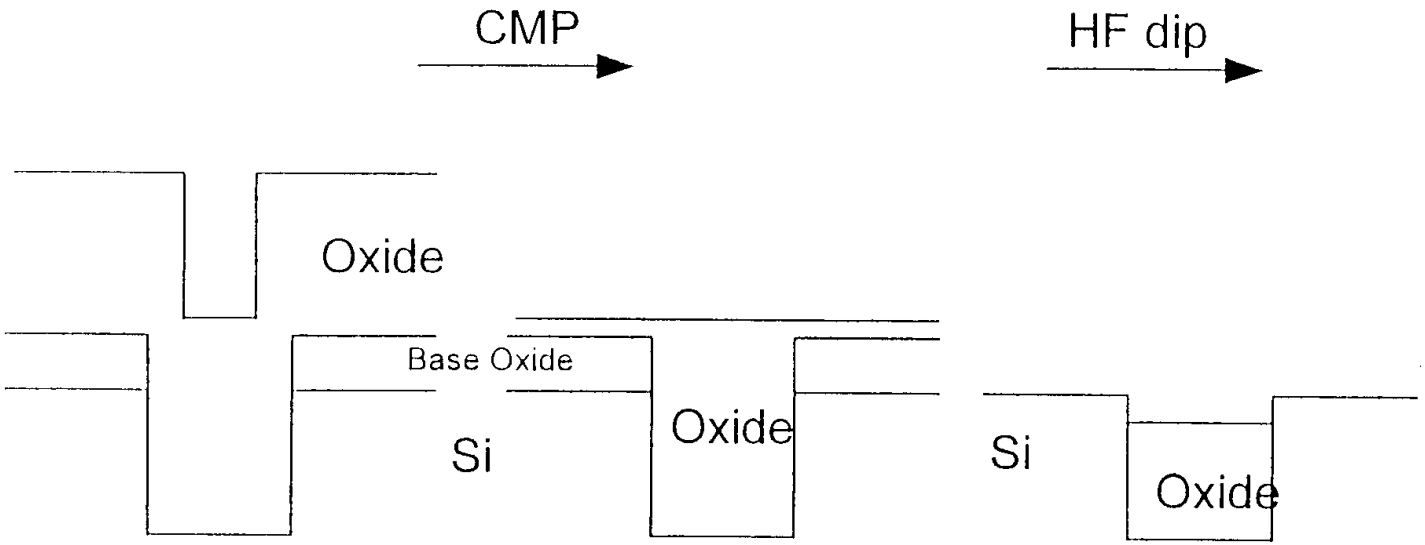
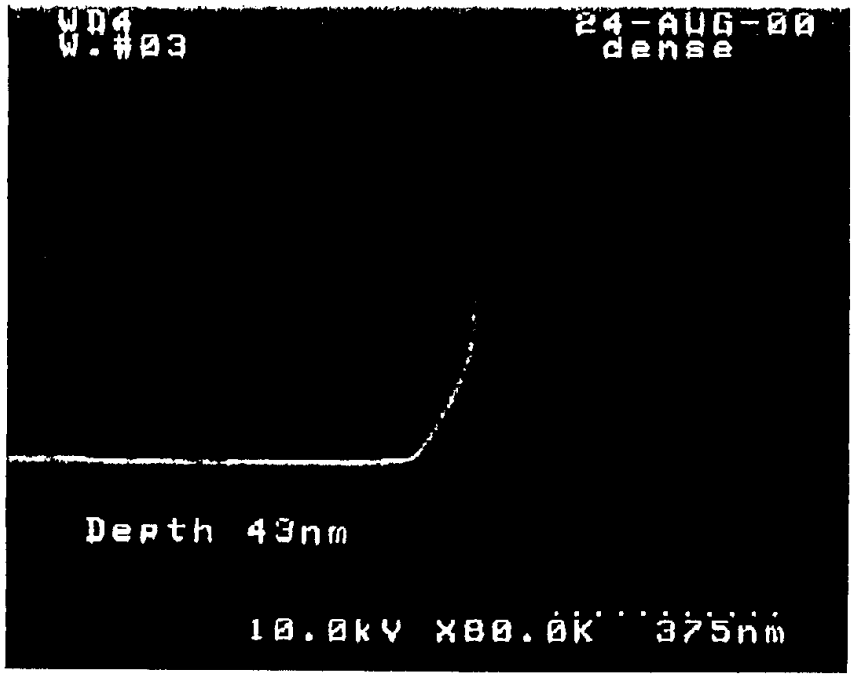


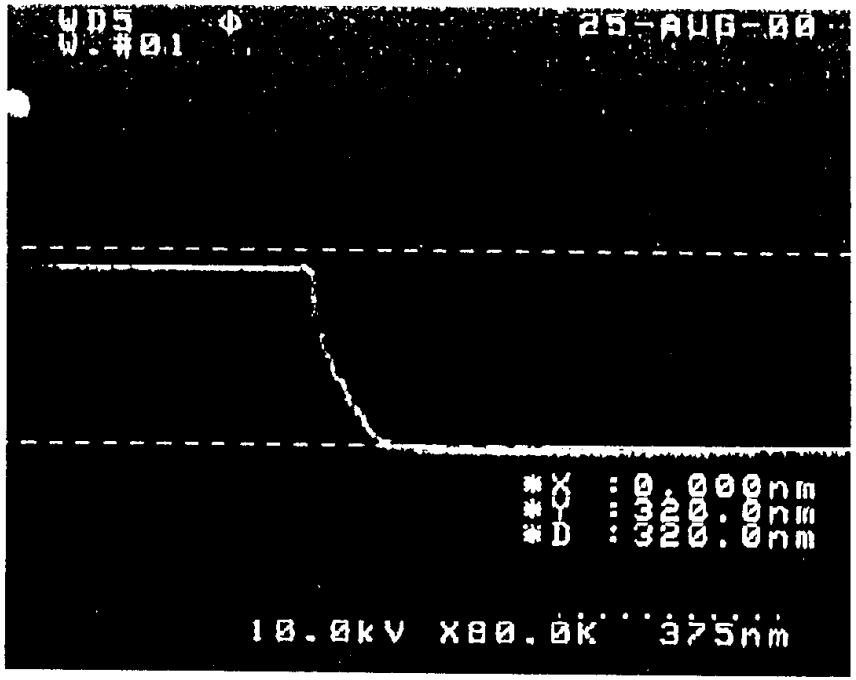
Exhibit A- page 8

Method of Making STI

Exhibit A- page 9

Option 1





Option 2

- Use doped oxide to increase selectivity during wet Dip
- polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height

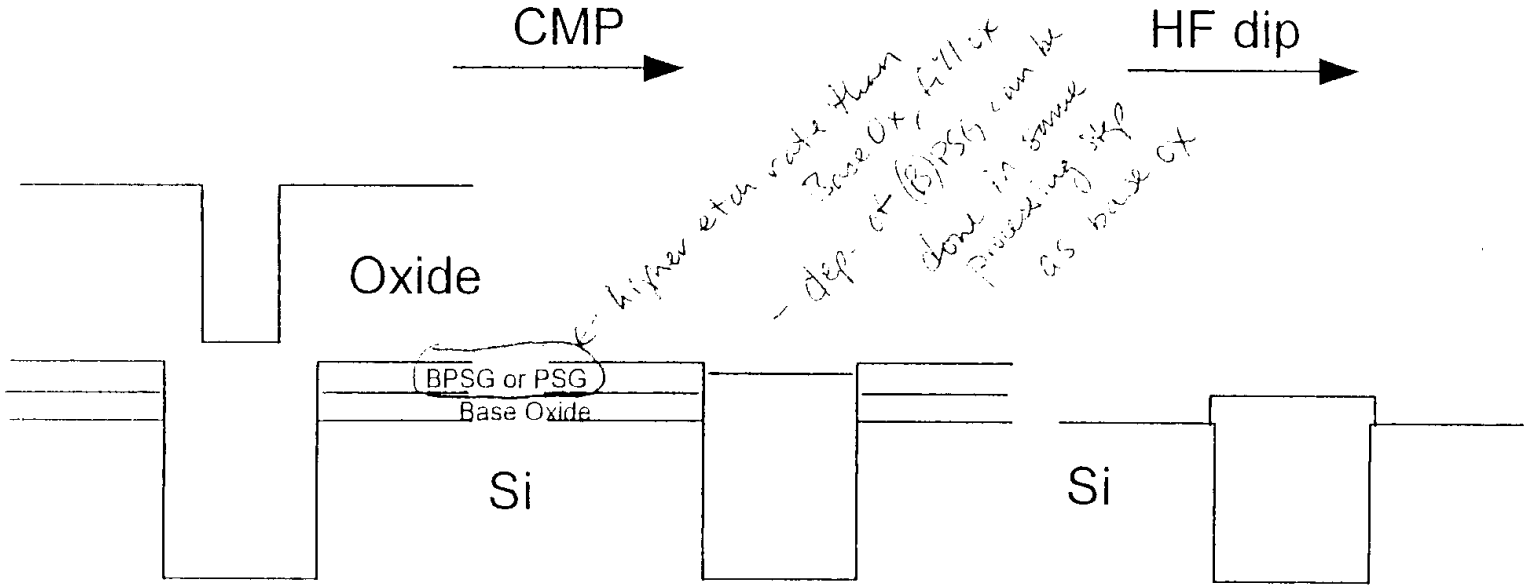


Exhibit A - page 10

Option 3

- Use thin Nitride
- polish to flatness - Fixed Abrasive ,stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step hieght

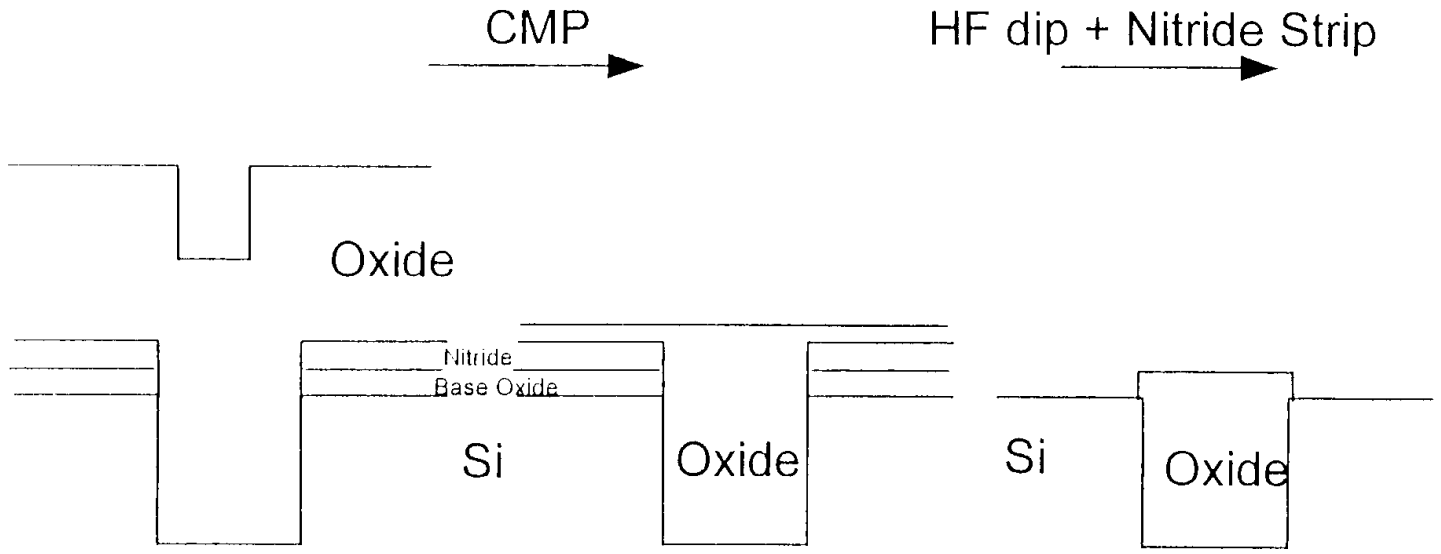


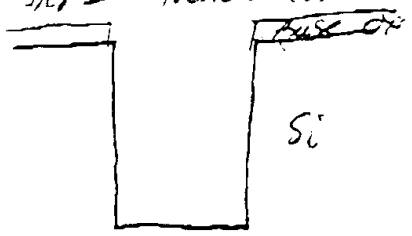
Exhibit A- page 11

STI

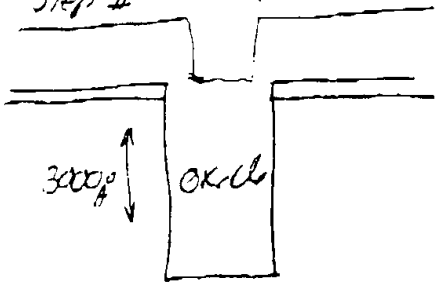
method of making shallow trench isolation structure with no/or thin nitride CMP stop.

① No Nitride - using Fixed Abrasive
Proposed by Steven Hedgepeth 10/15/99.

Step I trench definition



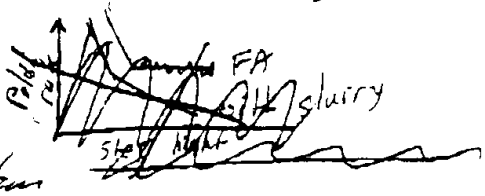
Step II - oxide dep using:
HDP
PECVD
APCVD

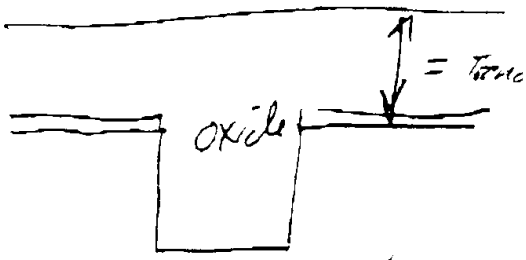


in step II
need to deposit trench depth + trench depth variation

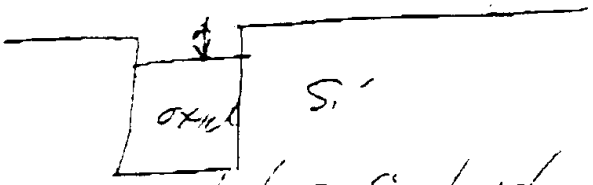
step III Polish

due to Fixed Abrasive properties CMP will self planarize once flatness is achieved.





step IV oxide Strip



Strip will result in oxide below Si level

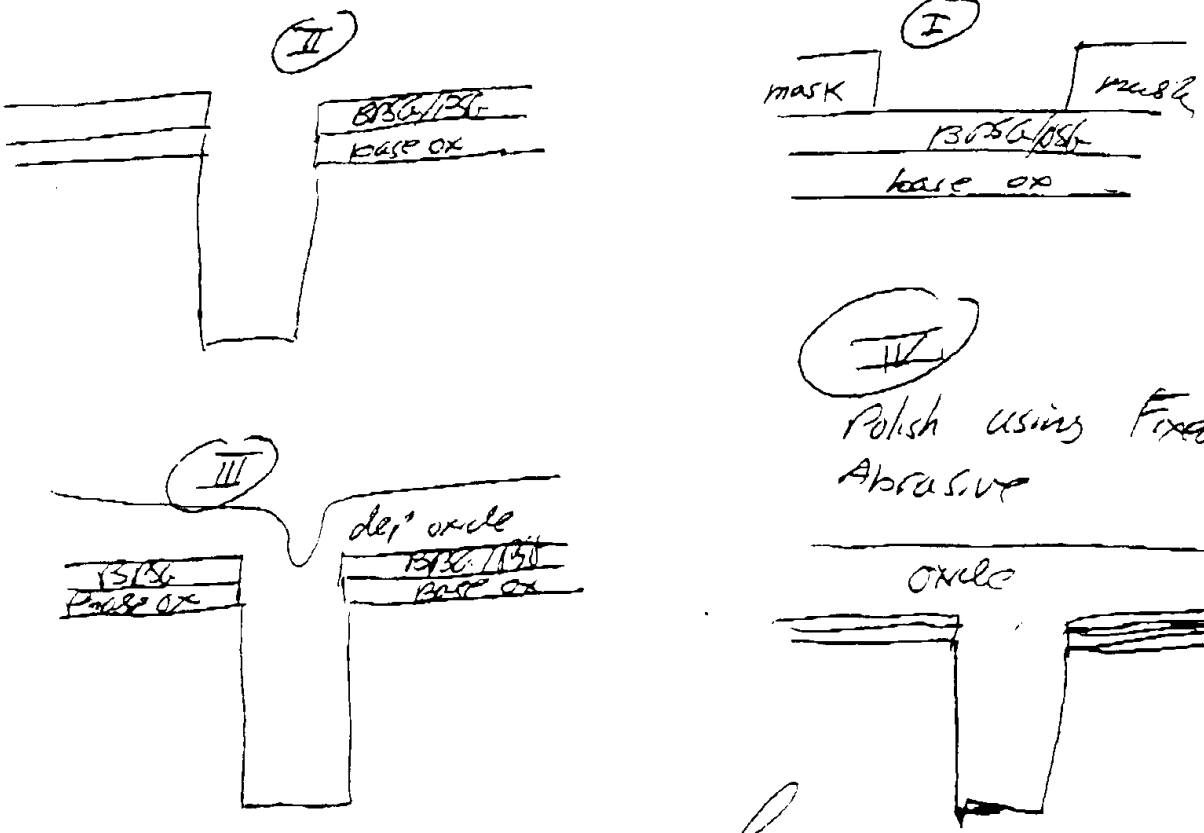
Steven Hedgepeth, Ramkumar, Bill Keating, Nick Colburn
S. Hedgepeth 11/15/99
N. Bhosle 11/15/99

Exhibit B- page 1

STI

as long as Trench depth variation as controlled below a certain number ie ± 500 Å then polish can be done without nitride layer.

(2) 2nd Method use of PSG/BPSG layer as a base oxide or on top of pad oxide



Bill Kouthey : B.K.

S. Hedges

Main Block

11/15/99

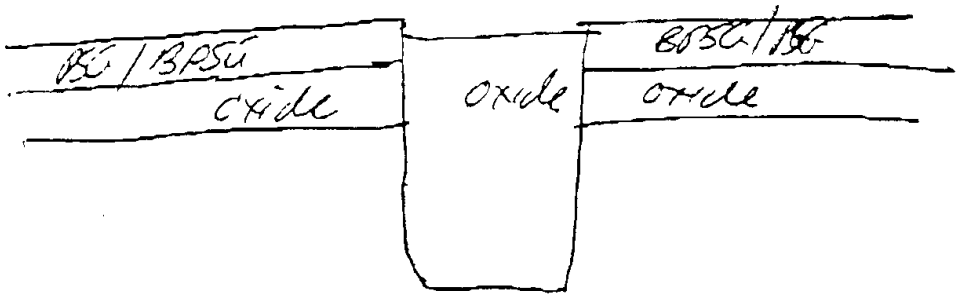
11/15/99

Exhibit B- page 2

~~Strip Oxide back to BPSG~~

Polish Back to BPSG layer

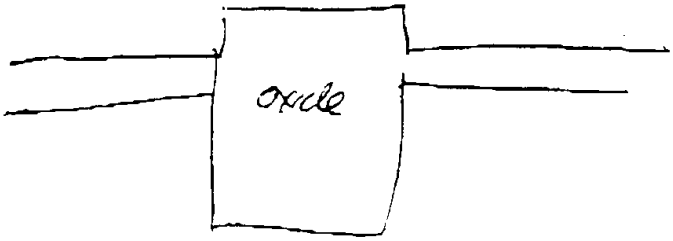
strip



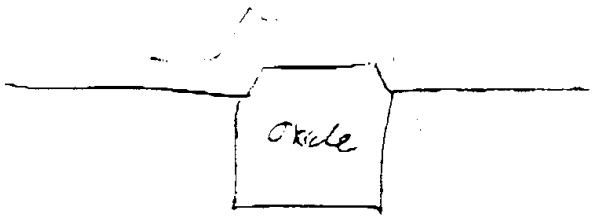
use act strip BPSG ER is N 50 time

thermal oxide rate so oxide will be

after strip I



after strip II



Bill Kountz Hyde Collins

S. Hedges
DA. - IDa.

11/15/89
11-15-89

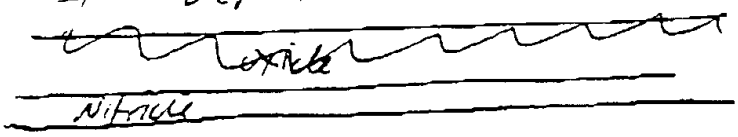
Exhibit B- page 3

STI

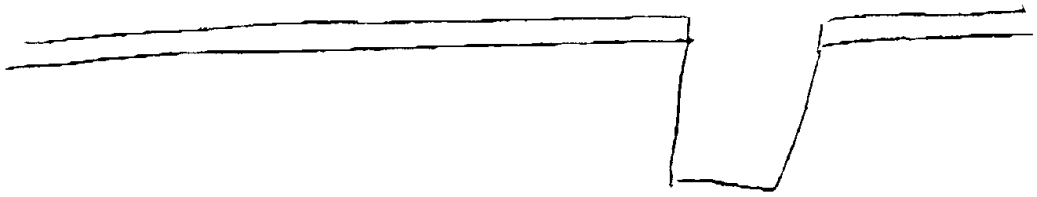
(3) use thin Nitride for STI

Nitride is used only as a means to determin oxide height above Si

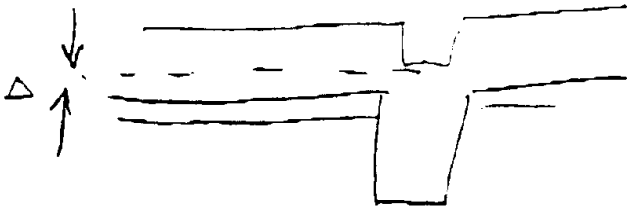
I dep Thin Nitride



II mask and etch



III dep HDP oxide or PECVD oxide or APCVD oxide



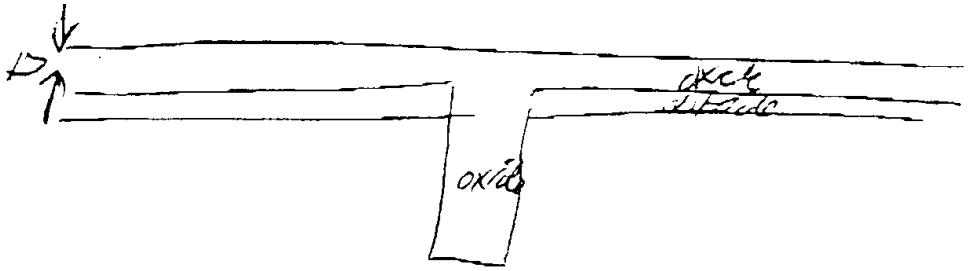
Thickness is targeted to achieve planarity at Δ Å above Si

Bill Kaufney - Idea by
S. Hedges
Alan Bloom

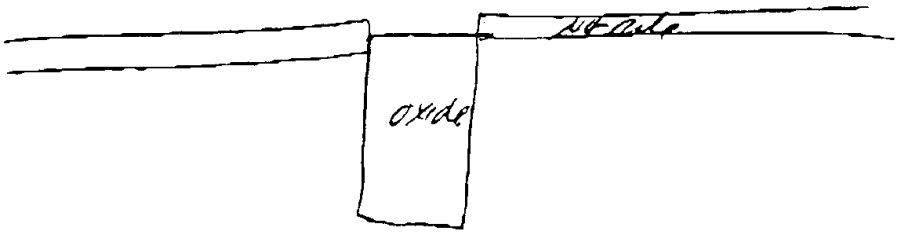
11/15/99
11/15/99

Exhibit B- page 4

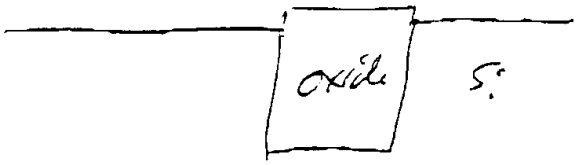
~~II~~ CMP



V act strip of oxide



VI nitride strip



Bill Kordzey Kyle Gilbert
S. Hedges
Alan Blum

11/15/99
11/15/99

Exhibit B- page 5

PATENT
5298-04700/PM00028

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

Serial No.: 09/846,119

Filed: April 30, 2001

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§ Group Art Unit: 1763
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§ Examiner: Goudreau, G.
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CERTIFICATE OF MAILING
37 C.F.R. § 1.18

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

Date Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, Steven Hedayati, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.

2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

CONCEPTION

3. As supported below, I, along with Yitzhak Gilboa, William W.C. Koutny, Jr. and Krishnaswamy Ramkumar, conceived of the subject matter claimed in the present application within the United States before June of 2000. The subject matter includes a method for forming a structure within a trench of a semiconductor topography.

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REDUCTION TO PRACTICE AND DILIGENCE

8. From at least a time just prior to June of 2000 through the filing of the application on April 30, 2001, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to June of 2000 through the filing of the application on April 30, 2001.

9. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to June of 2000 through the filing of the application on April 30, 2001.

10. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

_____

Steven Hedayati

Date: _____

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. **INVENTOR(S)** DISCLOSURE NO PM00028

***

A. Name YITZHAK GUSAT CY Initials YEG Empl. No. 7395 Ext. No. 2719

Citizenship U.S.A. Dept # 208 Home Phone No. 408-253-3567

Home Mailing Address 1761 HERON AVE SUNNYVALE CA 94087

***

B. Name William Hoatzey CY Initials B/K Empl. No 135 Ext. No. 2673

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Home Mailing Address 2555 Homestead #45 Santa Clara, CA 95051
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***

C. Name Steven Healyati CY Initials SSH Empl. No. 8584 Ext. No. 4556

Citizenship US Dept # 3168 Home Phone No. 408-927-0187

Home Mailing Address 1246 Valley Quail Circle San Jose CA 95120

2. **TITLE OF INVENTION** Method of making Shallow trench isolation Structure

3. **CONCEPTION OF INVENTION**

A. Date of first drawing or drawings Redacted
Where can first drawing be found Redacted

B. Date of first written description Redacted
Where is description found Redacted

C. Date of first oral disclosure to others Redacted
To whom? Discussed with KTR, SSH, B/K

4. **CONSTRUCTION OF DEVICE**

A. Date Completed _____
B. Was prototype made? _____
C. By whom made? _____
D. Where can the prototype be found? _____

Inventor(s) _____ Date 8/24/00

Inventor(s) _____ Date 8/24/00

Inventor(s) _____ Date 8/24/00

Witnessed, Read, and Understood by: _____ Date 8/24/00

Witnessed, Read, and Understood by: _____ Date 8/24/00
(Each page upon which information is entered should be signed and witnessed.)

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. **INVENTOR(S)** DISCLOSURE NO _____

***

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Citizenship INDIAN Dept # 3108 Home Phone No. (408) 255-1031

Home Mailing Address 1193 LYNBROOK WAY ; SAN JOSE ; CA 95129

***

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____

Citizenship _____ Dept # _____ Home Phone No. _____

Home Mailing Address _____

***

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____

Citizenship _____ Dept # _____ Home Phone No. _____

Home Mailing Address _____

2. **TITLE OF INVENTION** _____

3. **CONCEPTION OF INVENTION**

A. Date of first drawing or drawings _____
Where can first drawing be found _____

B. Date of first written description _____
Where is description found _____

C. Date of first oral disclosure to others _____
To whom? _____

4. **CONSTRUCTION OF DEVICE**

A. Date Completed _____
B. Was prototype made? _____
C. By whom made? _____
D. Where can the prototype be found? _____

Inventor(s) _____ Date _____

Inventor(s) _____ Date _____

Inventor(s) _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Each page upon which information is entered should be signed and witnessed.

Exhibit A- page 2

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

5. **TEST OF DEVICE**

A. Date: _____ Witness(es): _____

B. Results: _____

6. **SALE**

A. Was invention sold or offered for sale? Yes___ No✓
B. Was invention used to make, assemble or test a commercial product? Yes___ No✓
C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes___ No✓
D. Actual or estimated date of first sale, offer or commercial use _____
E. Is invention part of a product for which there is a data sheet? Yes___ No✓ (If yes, attach a copy)
F. Actual or estimated date of publication, release or availability of data sheet _____

7. **USE**

A. Is invention presently being used? Yes_____ No✓
***

B. In what product or process is invention presently being used?
***

_____

Are there specific plans for its use in near future? In what products or processes?

RAM-D

8. **RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS**

5,972,792 / 4010573 and 5,782,675 / 5919082

4393627 /

9. **WAS INVENTION** Conceived (Yes____ (No✓ Constructed (Yes____ (No✓ Tested (Yes____ (No✓ during performance of Government Contract?

Contract Number _____
(Give Full Contract Number)

==========

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventor(s) _____ Date 8/12/02

Inventor(s) _____ Date 8/12/02

Inventor(s) _____ Date 8/24/02

Witnessed, Read, and Understood by: _____ Date 8/24/02

Witnessed, Read, and Understood by: _____ Date 8/24/02

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 3

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
2. Describe old technology, if any, for performing the function of the invention. Provide references, if available
3. Indicate the disadvantages of the old technology.
4. Describe your invention and its construction, showing the changes, additions and improvements over the old method
5. Give details of its operation (i.e., how is your invention used?), if not already described under 4.
6. State the advantages of your invention over what has been done before.
7. Indicate any alternate component(s) and/or method(s) of construction.
8. If a joint invention, indicate what contribution was made by each inventor.
9. Describe the features that are believed to be new.
10. State opinion of relative value of invention.

***

11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

==========

1. The purpose of the invention is to improve the manufacturability of STI and reduce cost, this is done by reducing processing steps

2. Current technology (A7-1.0 TDK) calls for the following steps:

Inventor(s) _____ Date 8/24/00

Inventor(s) _____ Date 8/24/00

Inventor(s) _____ Date 8/24/00

Witnessed, Read, and Understood by: _____ Date 8/24/00

Witnessed, Read, and Understood by: A. Sadigh Date 8/24/00

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 4

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

(3.) Disadvantages addressed by invention:

1. Thick nitride-layer required to overcome STI dishing in Stacy CMP process. Thin nitride can reduce stress defects.
2. Additional etch required to Etch nitride
3. Extra step after nitride strip which can result in Stacy stringer
4. Trench fill deposition to overcome step induced by nitride.

(4) The current invention has three options with using Fixed abrasive polish as the ~~polish~~ method of polish. The main advantage of fixed abrasive is the negligible amount of dishing compared to conventional slurry process. The second advantage, self planarization, can reduce thickness of film

Option I – No nitride hard mask

In this option, no nitride hard mask. Following the core trench etch, strip resist and clean the wafer, deposit thin trench liner oxide to protect the trench and across the desired thickness of the trench + trench depth variation. After oxide deposition, the wafer is ready for fixed abrasive polish. A residual thickness of 0 – 500 Å. The last step comprises of a wet chemical etch to remove the oxide liner and the pad oxide. The process flow

Inventors: _____ Date _____

Inventors: _____ Date _____

Inventors: _____ Date _____

Witnessed, Read and Understood by: _____ Date _____

Witnessed, Read and Understood by: _____ Date _____

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 5

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

option II - Deposit Thin Nitride -

grow base oxide, grow thin layer of Nitride (0-500 Å) expose field oxide, etch trench, Deposit Nitride, polish down to ~~nitride~~ stop on oxide at a predetermined residual oxide where the nitride stop. Strip Remaining oxide, Strip Remaining nitride.

option III

grow base oxide, deposit BPSG/USG, expose field, etch trench, deposit thin oxide, which is BPSG/USG layer, use wet strip to remove remaining BPSG, use wet/dry wet strip to remove oxide, due to use of etch rate selectivities of BPSG to thin oxide to form stable field, Resulting, perform strip of sacrificial oxide, Nitride strip,

(6) - Trim overhangs of one of poly-layers of poly-oxide allowing the use of one of the poly layers,

(7) - Perform a trench etch, deposit field oxide, planarize, leaving field oxide for alignment + isolation steps.

Inventor(s) _____ Date _____

Inventor(s) _____ Date _____

Inventor(s) _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

(Each page upon which information is entered should be signed and witnessed.)

Exhibit A - page 6

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

(8) equal consumption

(9) Fixed abrasive polish, no polish stop, different polish stops

(10) - Invention will enable reduction of cost of ownership compared to Sloy.
- enable STI polish without requirement of reverse mask.
- enable STI polish with reduced step height budget required for 193 nm lithography.

Inventor(s) _____ Date _____

Inventor(s) _____ Date _____

Inventor(s) _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____
(Each page upon which information is entered should be signed and witnessed.)

Option 1

- No Nitride HM
- Stop after flatness - fixed abrasive
- Wet dip to below Si

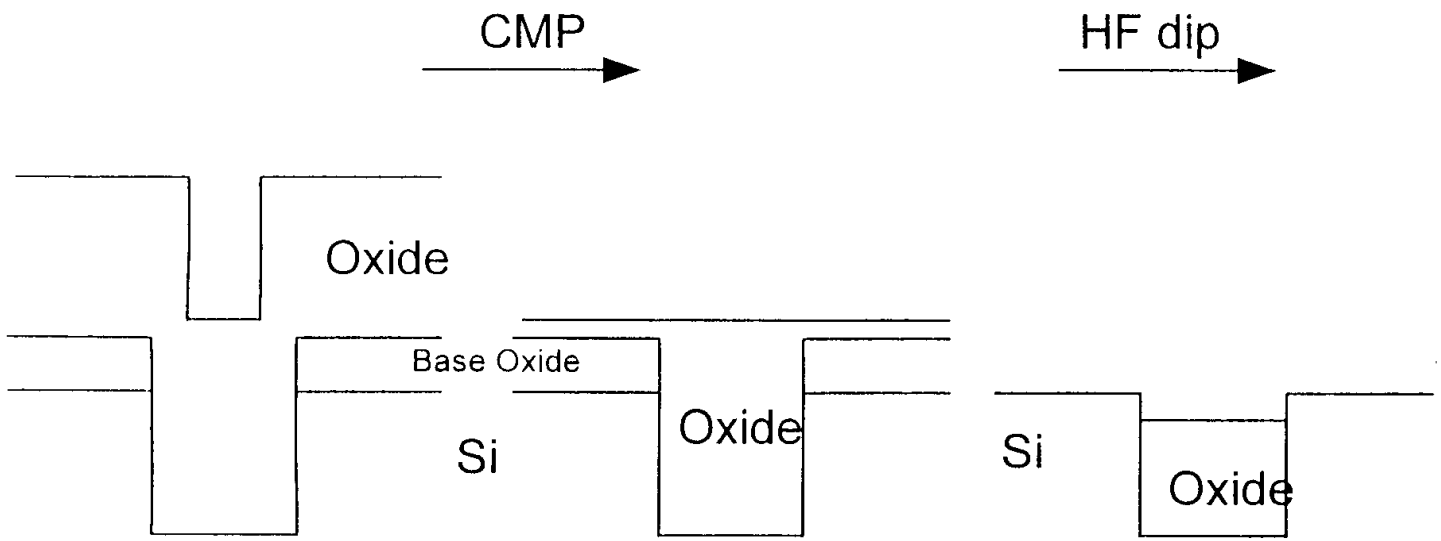
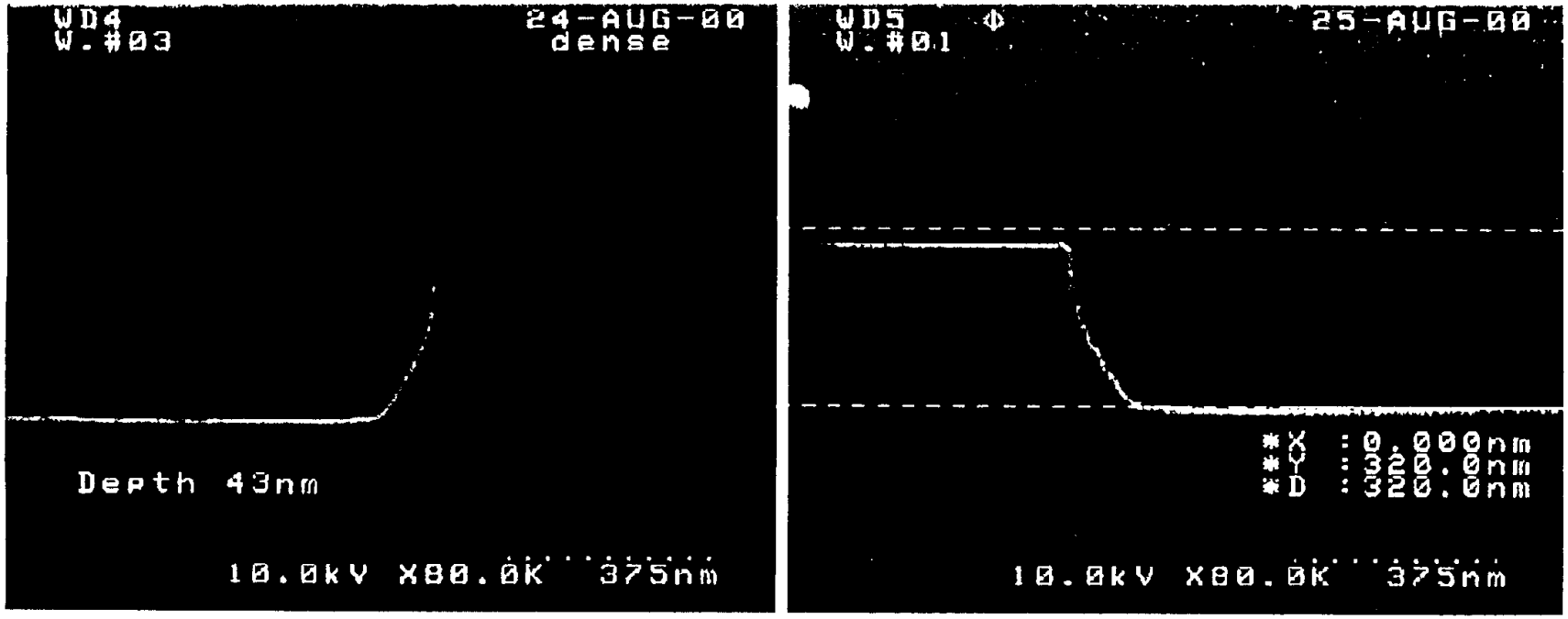


Exhibit A- page 8

Method of Making STI

Exhibit A- page 9

Option 1



Option 2

- Use doped oxide to increase selectivity during wet Dip
- polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height

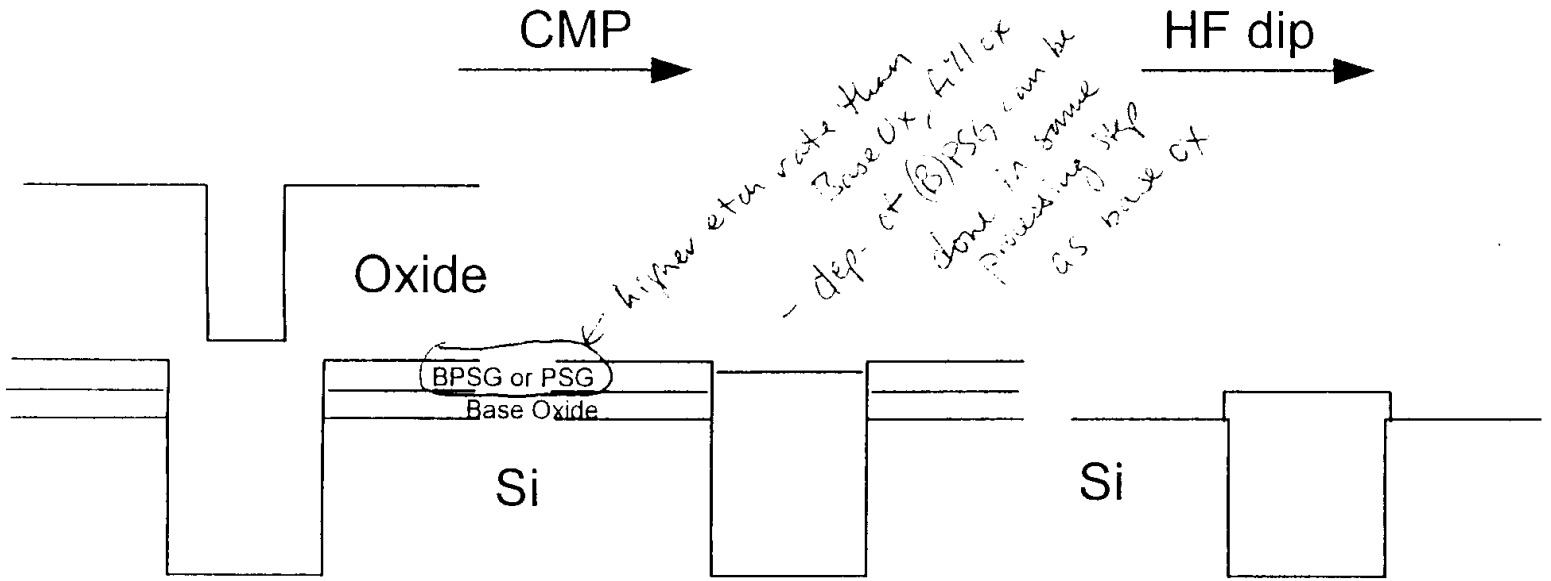


Exhibit A - page 10

Option 3

← old Nit: thick (~2000 Å) to act as CMP polish stop

- Use thin Nitride
- polish to flatness - Fixed Abrasive ,stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step hieght

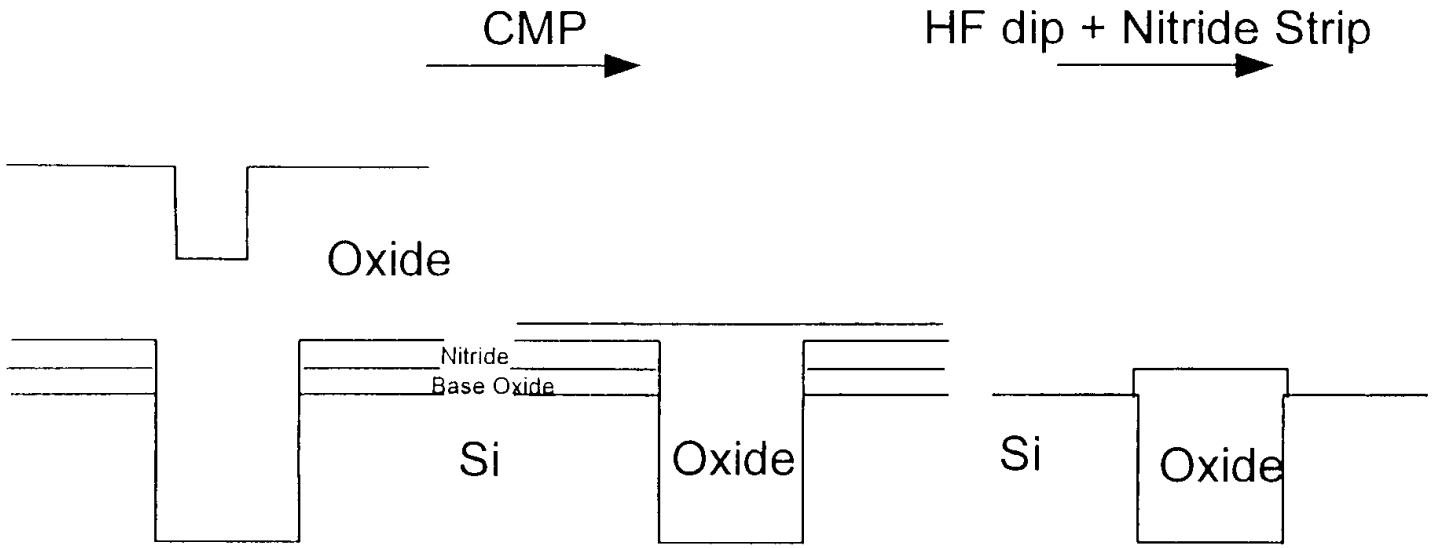
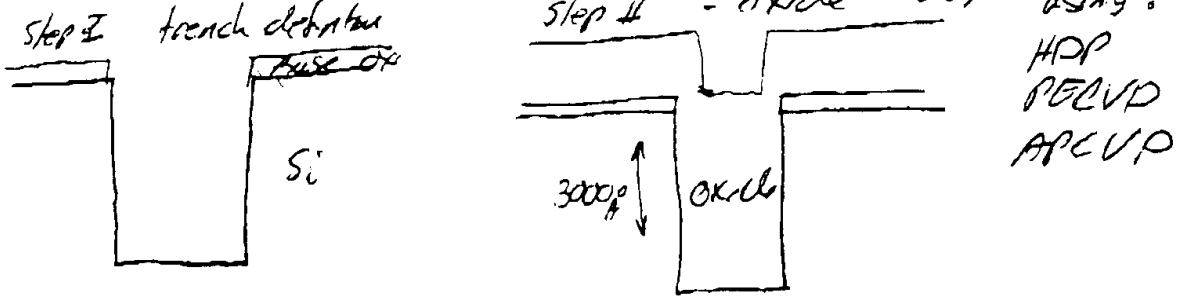


Exhibit A - page 11

STI

Method of making shallow trench isolation structure with no/or thin nitride CMP stop.

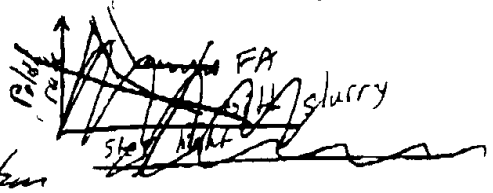
(1) No Nitride - using Fixed Abrasive
Proposed by Steven Hedegaard 10/15/99

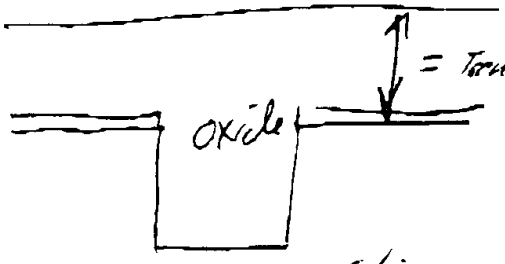


in step II
need to deposit trench depth + trench depth variation

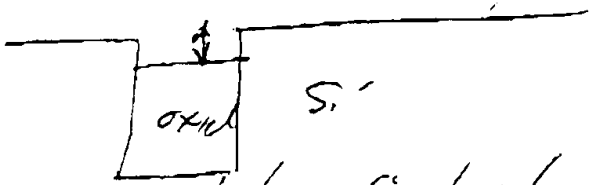
step III Polish

due to Fixed Abrasive properties CMP will self planarize once flatness is achieved.





step HF oxide Strip



Strip will result in oxide below Si level

Steven Hedegaard, Ramkumar, Bill Keating, Nick Gilbert

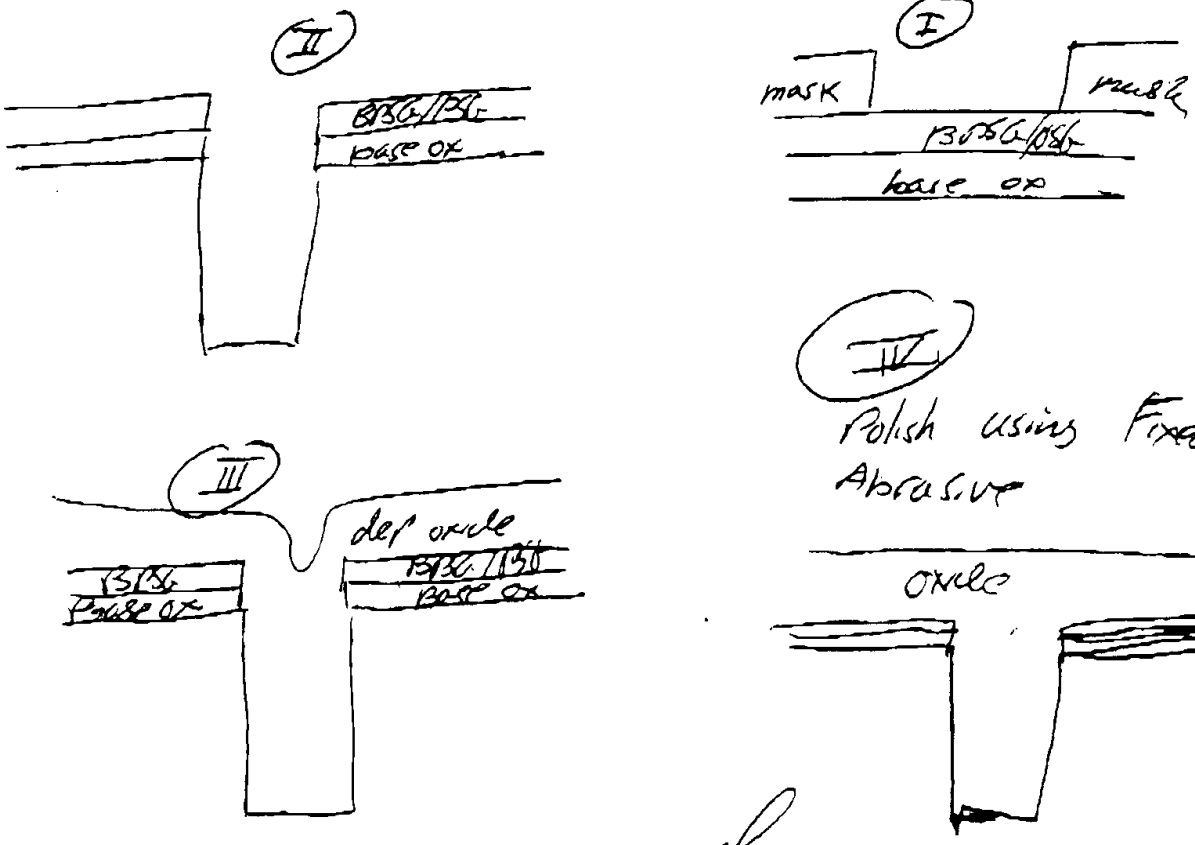
S. Hedegaard 11/15/99
N. Bloise 11/15/99

Exhibit B- page 1

STI

as long as Trench depth variation is controled bellow a certain number ie ± 500 Å then polish can be done without nitride layer.

(2) 2nd Method use of PSG/BPSG layer as a bas oxide or on top of pad oxide



Bill Kouthoy

S. Hedges

Alan Block

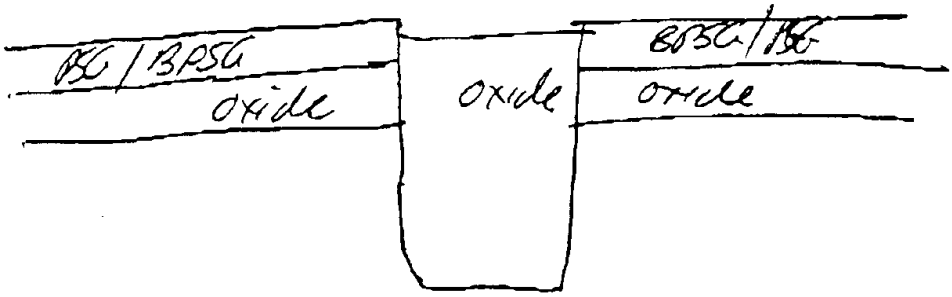
11/15/99

11/15/99

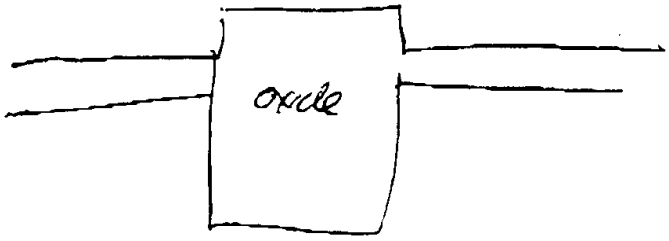
Exhibit B- page 2

~~strip oxide back to BPSG~~

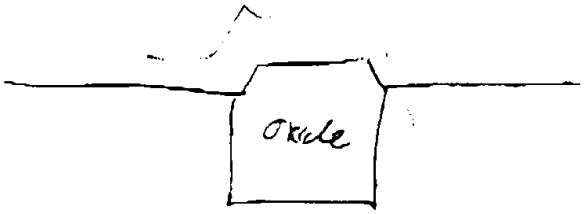
Polish Back to BPSG layer strip



use act strip BPSG ER is N 50 time thermal oxide rate so roughness will be after strip I



after strip II



Bill Kountz Pete Cotton

S. Hedges

11/15/99

11-15-99

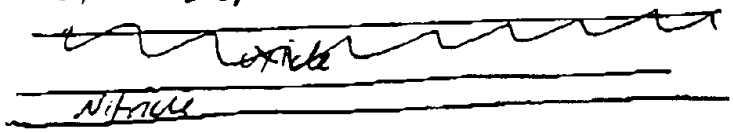
Exhibit B- page 3

STC

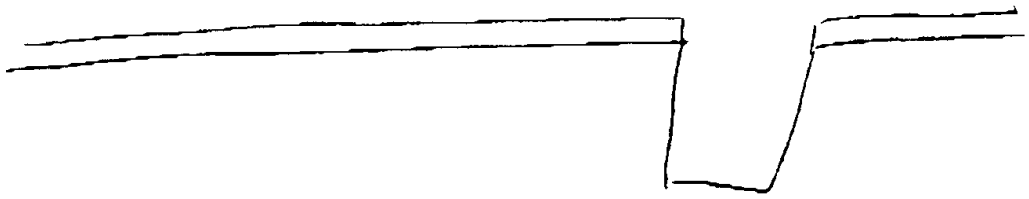
(3) use thin Nitride for STC

Nitride is used only as a means to determin oxide hight above Si

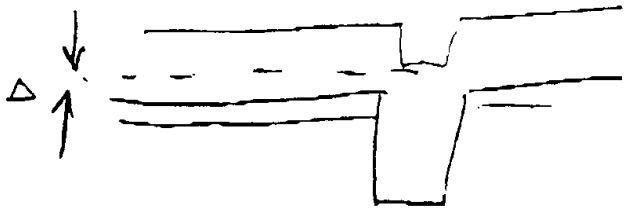
I dep Thin Nitride



II mask and etch



III dep HDP oxide or PECVD oxide or APCVD oxide



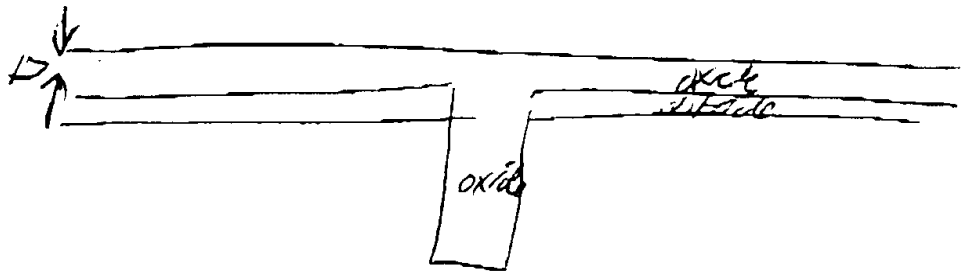
Thickness is targeted to achieve planarity at Δ Å above Si

Bill Kountney
S Hedges
Alan Boone

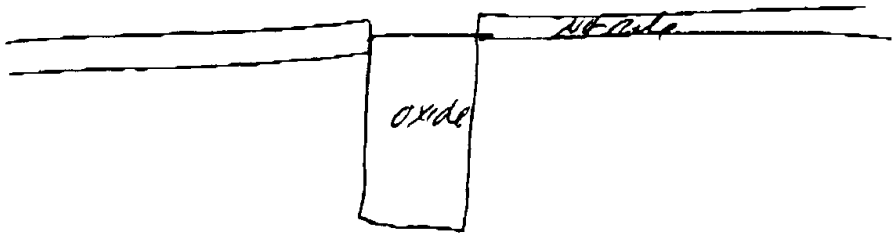
11/15/99
11/15/99

Exhibit B- page 4

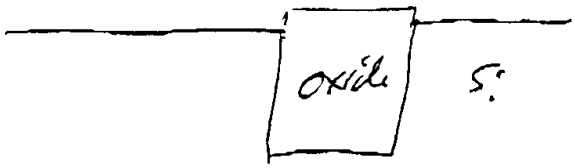
~~IV~~ CMP



V wet strip of oxide



VI nitride strip



Bill Kovarsky Kyle Gilbert 11/15/99
S. Hedges Alan Blum 11/15/99

Exhibit B- page 5

PATENT
5298-04700/PM00028

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

Serial No.: 09/846,119

Filed: April 30, 2001

For: METHOD OF MAKING A PLANARIZED SEMICONDUCTOR STRUCTURE

Group Art Unit: 1763

Examiner: Goudreau, G.

Atty. Dkt. No.: 5298-04700

CERTIFICATE OF MAILING
37 C.F.R. § 1.18

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

9-19-03
Date

Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, Krishnaswamy Ramkumar, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.

2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

CONCEPTION

3. As supported below, I, along with Yitzhak Gilboa, William W.C. Koutny, Jr. and Steven Hedayati, conceived of the subject matter claimed in the present application within the United States before June of 2000. The subject matter includes a method for forming a structure within a trench of a semiconductor topography.

4. Exhibit A attached hereto is a true copy of an invention disclosure form and attached pages which bear dates before June of 2000 corresponding to the conception of the invention. The actual dates for the first drawings, the first written description and first oral disclosure to others have been redacted.

5. Page 5 of Exhibit A describes the subject matter of the presently claimed case including the use of fixed abrasive polishing techniques to produce structures with a limited amount of dishing.

6. Exhibit B attached hereto is a true copy of a written description of the conceived subject matter, dated before June of 2000.

7. Page 2 of Exhibit B describes the subject matter of the rejected claims including the use of fixed abrasive polishing techniques to polish a layer deposited within a trench.

REDUCTION TO PRACTICE AND DILIGENCE

8. From at least a time just prior to June of 2000 through the filing of the application on April 30, 2001, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to June of 2000 through the filing of the application on April 30, 2001.

9. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to June of 2000 through the filing of the application on April 30, 2001.

10. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Krishnaswamy Ramkumar

Date: 1/19/03

CONLEY ROSE, P.C.

INTELLECTUAL PROPERTY LAW
INCLUDING
PATENTS, TRADEMARKS,
COPYRIGHTS AND
UNFAIR COMPETITION

A PROFESSIONAL CORPORATION
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KEVIN L. DAFFER
(512) 476-1400
kdaffer@conley-rose.com

5298-04700

August 21, 2003

Steven Hedayati
1240 Valley Quail Circle
San Jose, CA 95120

Via Certified Mail, RRR

Re: Declaration to Predate Reference with Regard to Cypress Patent Application PM00028

Dear Mr. Hedayati:

I am contacting you in regard to a patent application filed on behalf of Cypress Semiconductor Corporation. You are listed as a co-inventor of the invention, along with Yitzhak Gilboa, Krishnaswamy Ramkumar and William W. C. Koutny, Jr. The application is entitled "Method of Making a Planarized Semiconductor Substrate" and Cypress's reference number is PM00028. The application was filed on April 30, 2001.

We have received a rejection from the U.S. Patent and Trademark Office citing some patents and publications which teach some of the limitations claimed in the patent application. One of the references may be overcome by filing a declaration that the conception date of the invention is prior to the publication date of the cited reference. Enclosed herein is a copy of such a declaration. Please review, sign and return the enclosed declaration as soon as possible. Your immediate attention to this matter is appreciated.

I have also attached a copy of the invention disclosure form and copies of Yitzhak's lab notebook pertaining to the patent application. The documents will be filed with the declarations as Exhibits A and B, respectively. As noted in the declarations, the reference we are declaring to predate is an article in *Solid State Technology* entitled "Improved Planarization for STI with Fixed Abrasive Technology" by Vo et al., which was published in June of 2000. If you would like me to send you a copy of the article, please let me know.

Please do not hesitate to call me at (512) 703-1242 if you have any questions.

Very truly yours,

Kevin Daffer /S

Kevin L. Daffer

Enclosure

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S) DISCLOSURE NO PM00028

***

A. Name [illegible] CY Initials [illegible] Empl. No. [illegible] Ext. No. 2719

Citizenship U.S.A. Dept # [illegible] Home Phone No. 408-255-[illegible]

Home Mailing Address 1761 Herbert Ave Sunnyvale CA 94087

***

B. Name William Bintley CY Initials BK Empl. No 135 Ext. No. 2673

Citizenship [illegible] Dept # Home Phone No. 435-[illegible]

Home Mailing Address 2555 Homestead #45 Santa Clara, CA 95051
2555 Homestead 45 95051

***

C. Name Steven Hedges CY Initials SSH Empl. No. 8534 Ext. No. 4556

Citizenship US Dept # 3108 Home Phone No. 408-927-9187

Home Mailing Address 1242 Valley Quail Circle San Jose CA 95120

2. TITLE OF INVENTION Method of making Shallow trench isolation Structure

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings Redacted
Where can first drawing be found Redacted

B. Date of first written description Redacted
Where is description found Redacted

C. Date of first oral disclosure to others Redacted
To whom? Discussed with KTK SSH BK

4. CONSTRUCTION OF DEVICE

A. Date Completed
B. Was prototype made?
C. By whom made?
D. Where can the prototype be found?

Inventor's: [signature] Date 1/21/00

Inventor's: [signature] Date 5/24/00

Inventor's: [signature] Date 5/24/00

Witnessed, Read, and Understood by: [signature] Date 5/24/00

Witnessed, Read, and Understood by: [signature] Date 5/24/00

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 1

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S) DISCLOSURE NO _____

***

A. Name Ramkumar CY Initials KTR Empl. No. 3305 Ext. No. 2726

Citizenship INDIAN Dept # 3108 Home Phone No. (408) 255-1031

Home Mailing Address 1193 LYNBROOK WAY, SAN JOSE, CA 95129

***

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____

Citizenship _____ Dept # _____ Home Phone No. _____

Home Mailing Address _____

***

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____

Citizenship _____ Dept # _____ Home Phone No. _____

Home Mailing Address _____

2. TITLE OF INVENTION _____

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings _____
Where can first drawing be found _____

B. Date of first written description _____
Where is description found _____

C. Date of first oral disclosure to others _____
To whom? _____

4. CONSTRUCTION OF DEVICE

A. Date Completed _____
B. Was prototype made? _____
C. By whom made? _____
D. Where can the prototype be found? _____

Inventors: _____ Date _____

Inventors: _____ Date _____

Inventors: _____ Date _____

Witnessed, Read and Understood by _____ Date _____

Witnessed, Read and Understood by _____ Date _____

Each page upon which information is entered should be signed and witnessed.

Exhibit A- page 2

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

5. **TEST OF DEVICE**

A. Date: _____ Witness(es): _____

B. Results: _____

6. **SALE**

A. Was invention sold or offered for sale? Yes___ No✓
B. Was invention used to make, assemble or test a commercial product? Yes___ No✓
C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes___ No✓
D. Actual or estimated date of first sale, offer or commercial use _____
E. Is invention part of a product for which there is a data sheet? Yes___ No✓ (If yes, attach a copy)
F. Actual or estimated date of publication, release or availability of data sheet _____

7. **USE**

A. Is invention presently being used? Yes_____ No✓

***

B. In what product or process is invention presently being used?

***

_____

Are there specific plans for its use in near future? In what products or processes?

RAM-8

8. **RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS**

5,972,792 / 4010573 and 5782675 / 5919072

4395629 / [illegible]

9. **WAS INVENTION** Conceived (Yes____ (No✓ Constructed (Yes____ (No✓ Tested (Yes____ (No✓ during performance of Government Contract?

Contract Number _____
(Give Full Contract Number)

==========

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventor(s): [signature] Date [illegible]

Inventor(s): [signature] Date 6/20/00

Inventor(s): [signature] Date 3/24/00

Witnessed, Read, and Understood by: [signature] Date [illegible]

Witnessed, Read, and Understood by: [signature] Date [illegible]

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 3

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
2. Describe old technology, if any, for performing the function of the invention. Provide references, if available.
3. Indicate the disadvantages of the old technology.
4. Describe your invention and its construction, showing the changes, additions and improvements over the old method.
5. Give details of its operation (i.e., how is your invention used?), if not already described under 4.
6. State the advantages of your invention over what has been done before.
7. Indicate any alternate component(s) and/or method(s) of construction.
8. If a joint invention, indicate what contribution was made by each inventor.
9. Describe the features that are believed to be new.
10. State opinion of relative value of invention.

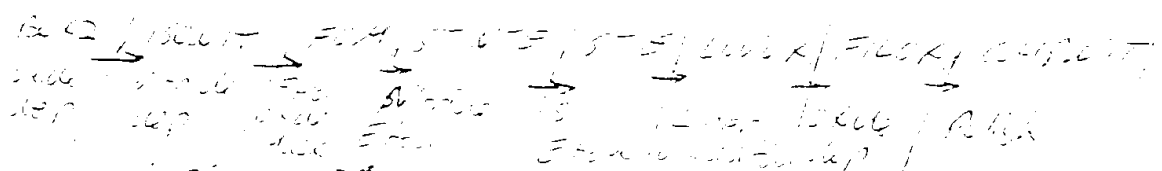
***

11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

==========

1. The purpose of the invention is to improve the manufacturability of STI and reduce cost, by eliminating processing steps

2. Current technology (0.7-1.0 TDR) calls for the following steps:



Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 4

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

(3.) Disadvantages addressed by invention:

1. Thick nitride layer required to overcome 500Å dishing in slurry CMP process. This nitride can induce stress defects.
2. Additional etch required to etch nitride
3. Oxide step after nitride strip which can result in poly stringers
4. Thicker oxide fill deposition to overcome step induced by nitride.

(4) The current invention has three options all using Fixed Abrasive polish as the ~~[illegible]~~ method of polish.
The main advantage of Fixed Abrasive is the negligible amount of dishing compared to conventional slurry process.
The second advantage is self planarization, no nitride required at [illegible]

Option I – No Nitride Hard mask

In this option no nitride film is used. Film is [illegible] on bare silicon. Trench etch [illegible] of one step [illegible] the trench is opened. After trench etch oxide fill [illegible] in the trench and across the [illegible] a thickness of the trench + trench depth variation. After oxide deposition the oxide is polished using Fixed Abrasive to a [illegible] thickness of 0–500Å.
The [illegible]
[illegible]

Inventor(s): [illegible signature] Date [illegible]
Inventor(s): [illegible signature] Date [illegible]
Inventor(s): [illegible signature] Date [illegible]
Witnessed, Read, and Understood by: [illegible signature] Date [illegible]
Witnessed, Read, and Understood by: [illegible signature] Date [illegible]
Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 5

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

option II - Deposit Thin Nitride -

grow base oxide grow thin layer of Nitride (~500Å) expose field oxide mask, Etch Nitride, Deposit fill oxide polish down to ~~nitride~~ stop on oxide at a predetermined residual oxide above the Nitride. Strip remaining oxide. Strip Remaining Nitride,

option III

grow base oxide deposit Nitride, expose resist Etch Nitride, deposit fill oxide, Etch to ~~Nitride~~ leave use wet strip to remove remaining Nitride, use dilute wet strip to remove oxide, time to wet Etch Rate differences of oxide to resist expose oxide to wet Etch Rate Nitride ~~to~~ to achieve step of the bottom oxide. Nitride Strip,

(6) - Deposition of Nitride Properties of the oxide by the use of the Nitride Nitride.

(7) - Deposition of the oxide Nitride, to the oxide Nitride Nitride Strip Nitride - Nitride Nitride.

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 6

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

(8) Equal consideration

(9) Fixed abrasive polish, no polish stop, oxide track polish stop

(10) - Invention will enable reduction of cost of ownership compared to slurry.
- enable STI polish without requirement of reverse mask.
- enable STI polish with reduced step height required for 193 nm lithography

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Witnessed, Read and Understood by: _____ Date _____

Witnessed, Read and Understood by: _____ Date _____
(Each page upon which information is entered should be signed and witnessed.)

Option 1

- No Nitride HM
- Stop after flatness - fixed abrasive
- Wet dip to below Si

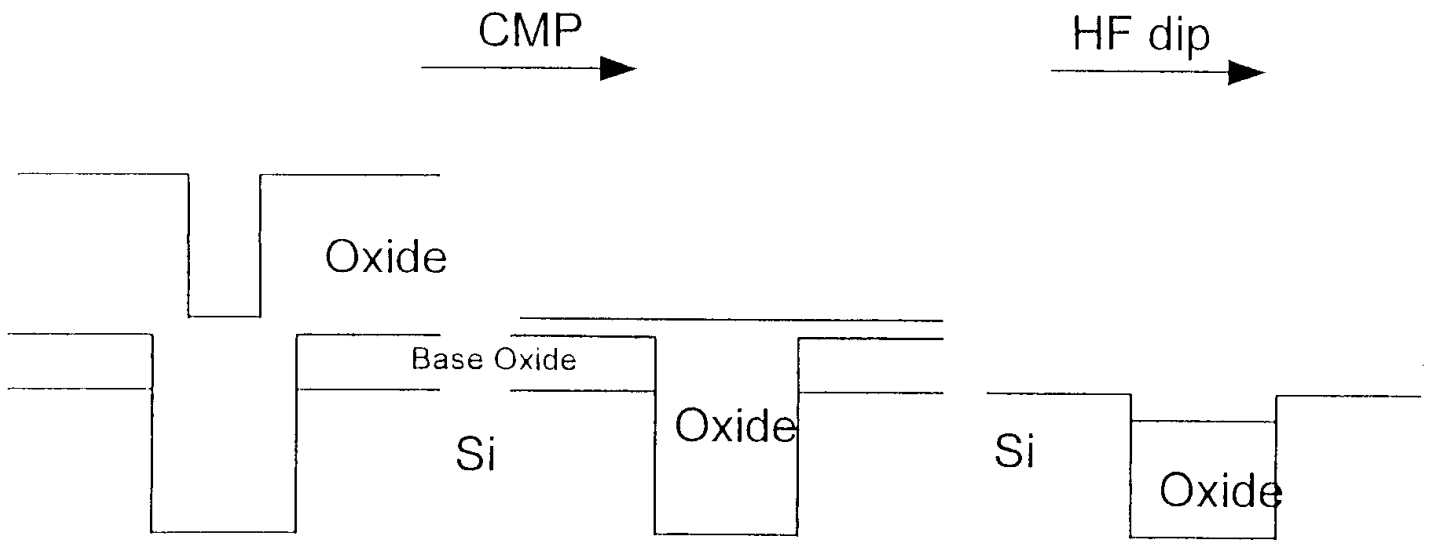
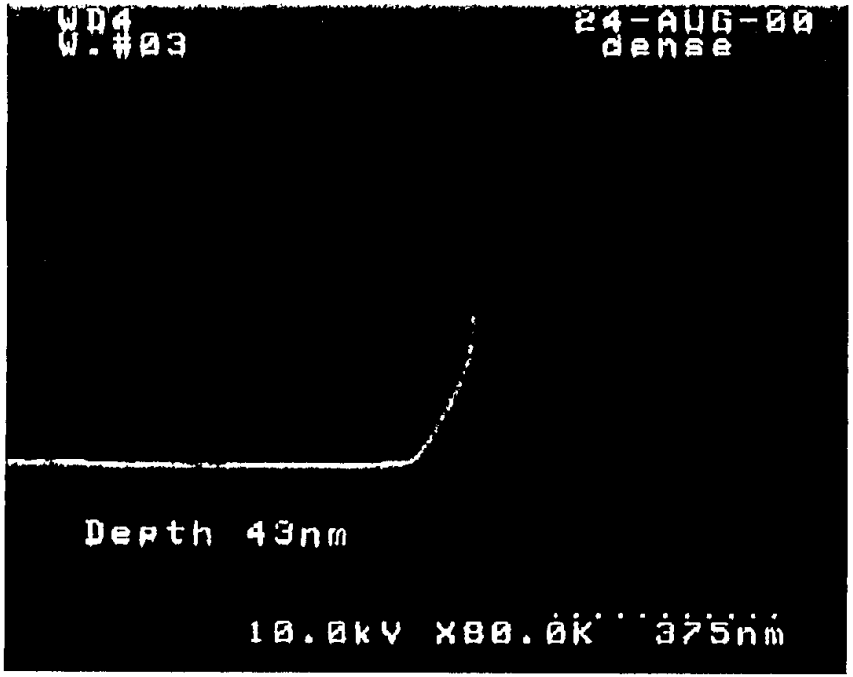


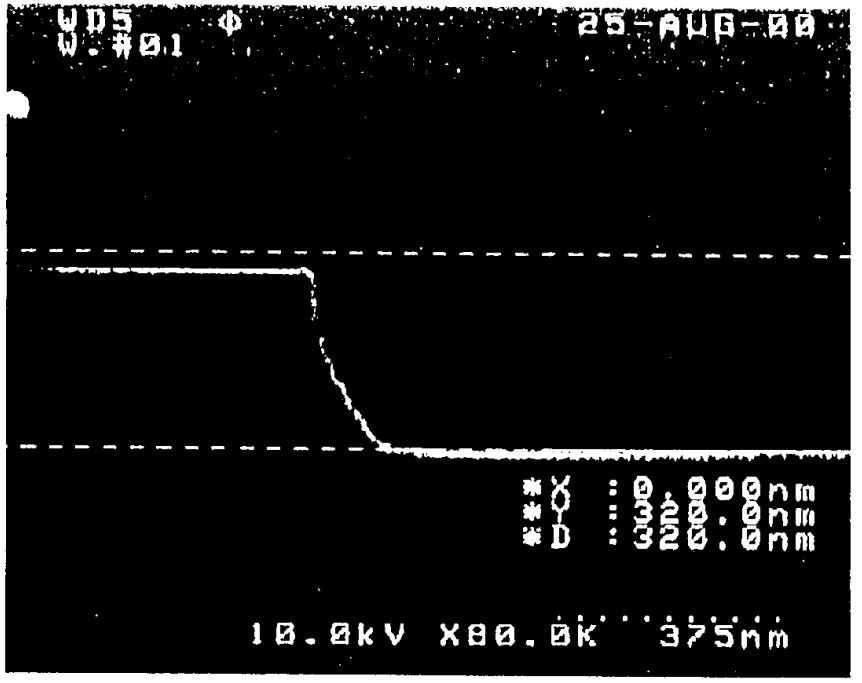
Exhibit A - page 8

Method of Making STI

Exhibit A- page 9

Option 1

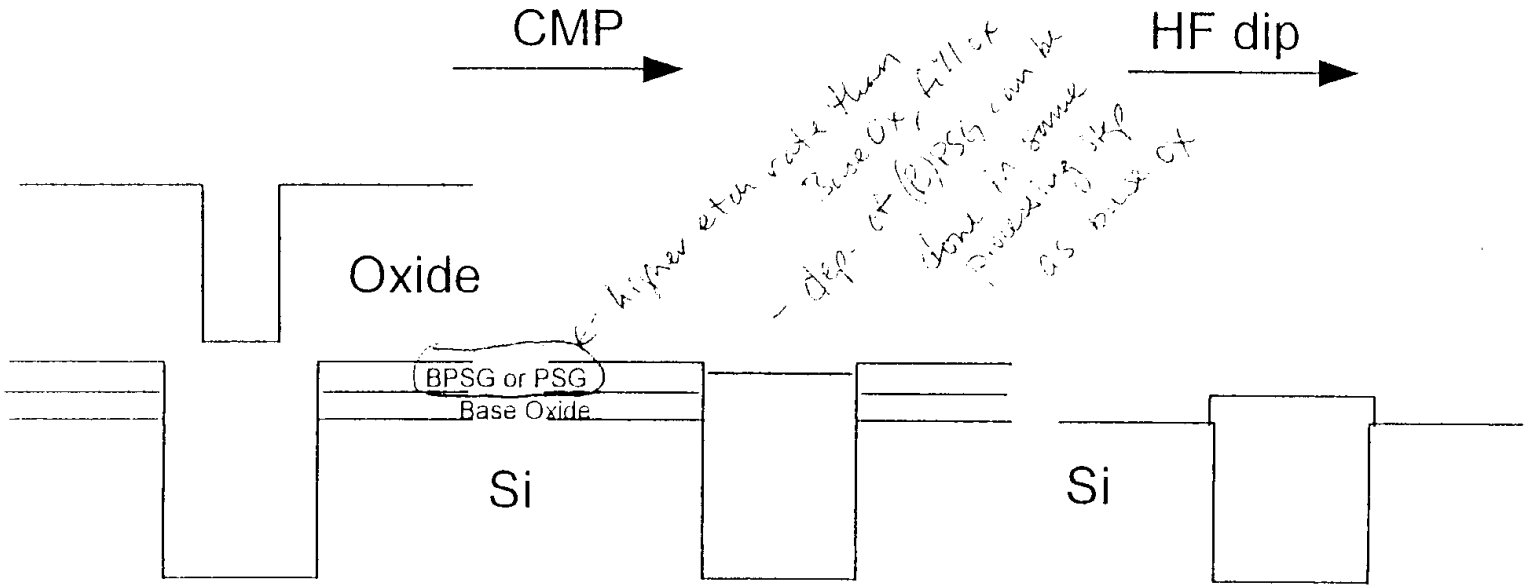




Option 2

Exhibit A - Page 10

- Use doped oxide to increase selectivity during wet Dip
- polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height



Option 3

- Use thin Nitride
- polish to flatness - Fixed Abrasive ,stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step hieght

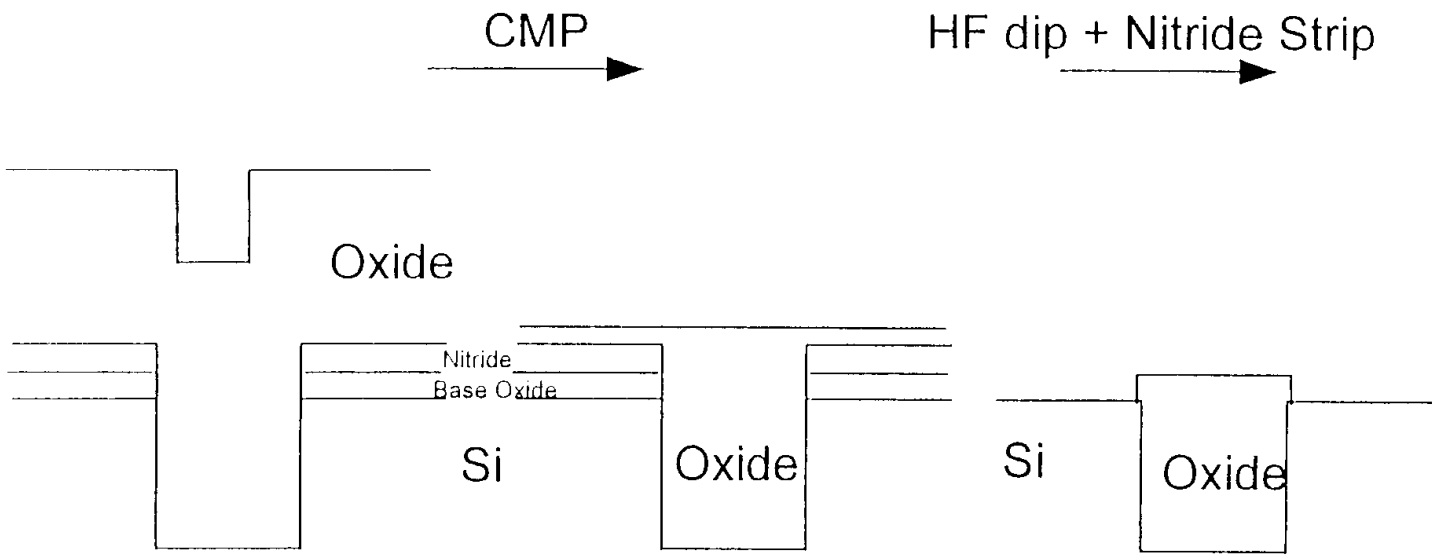


Exhibit A- page 11

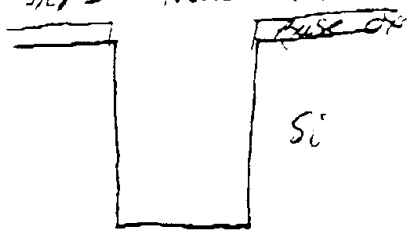
1

STI

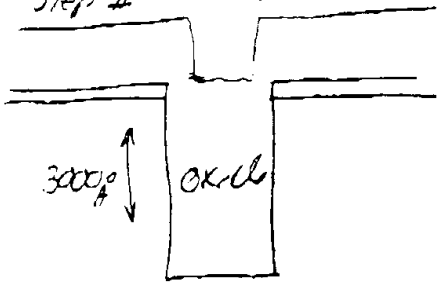
method of making shallow trench isolation structure with no/or thin nitride CMP stop.

(1) No Nitride - using Fixed Abrasive
Proposed by Steven Hedgepeth 10/15/99.

Step I trench definition



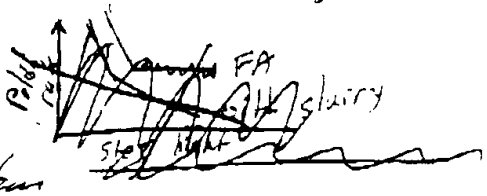
Step II - oxide dep using:
HDP
PECVD
APCVD

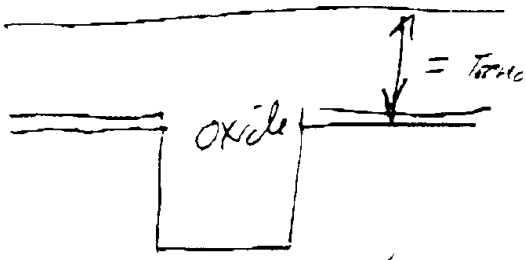


in step II
need to deposit trench depth + trench depth variation

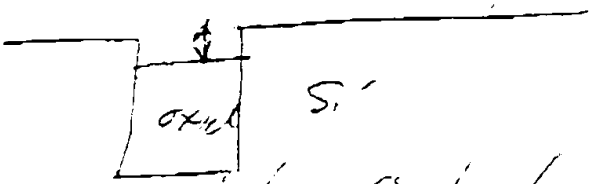
step III Polish

due to Fixed Abrasive properties CMP will self planarize once flatness is achieved.





step IV oxide Strip



Strip will result in oxide below Si level

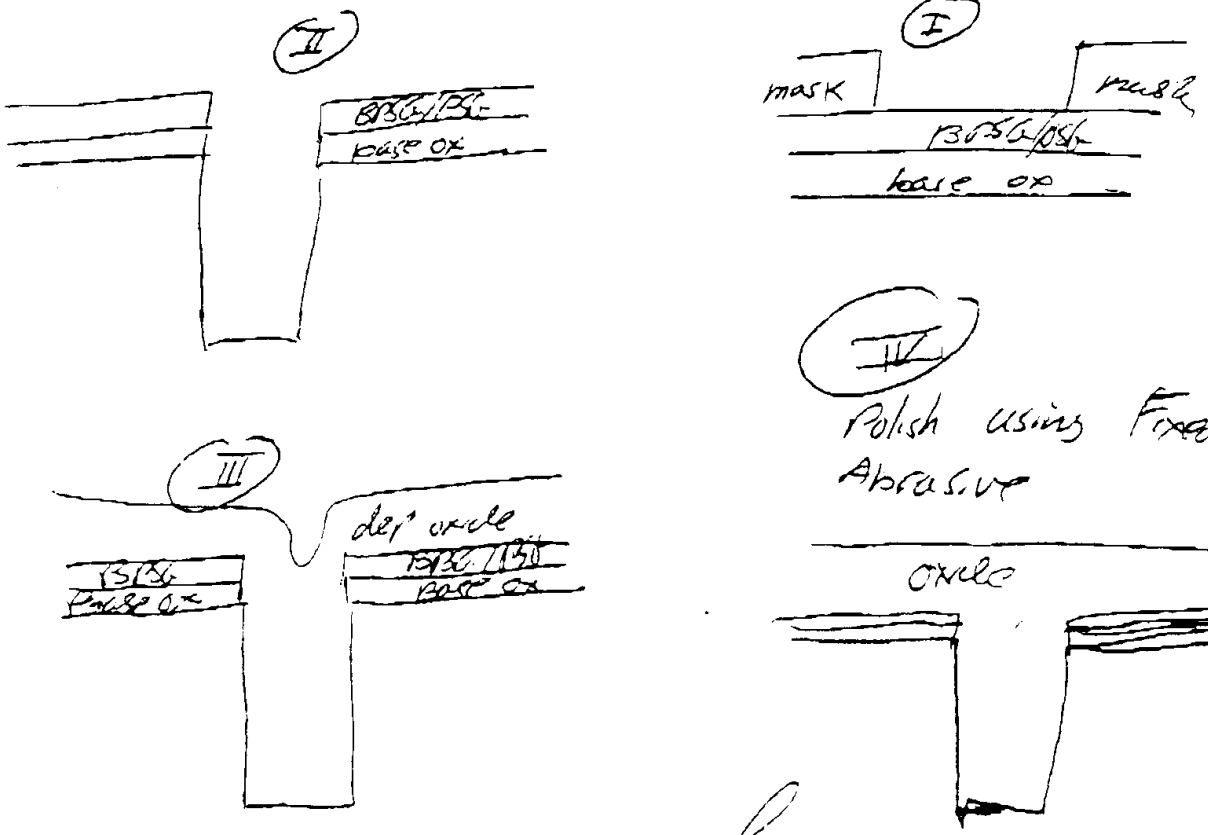
Steven Hedgepeth, Ramkumar, Bill Keating, Nick Gilbert
S. Hedgepeth 11/15/99
N. Gilbert 11/15/99

Exhibit B- page 1

STI

as long as Trench depth variation is controlled below a certain number ie ± 500 Å then polish can be done without nitride layer.

(2) 2nd method use of PS/BPSG layer as a base oxide or on top of pad oxide



Bill Kouthoy

S. Hedges

Mask Block

11/15/99

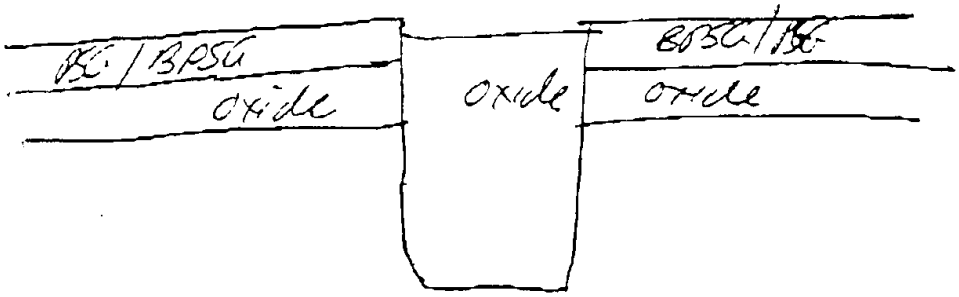
11/15/99

Exhibit B- page 2

~~Strip Oxide back to BPSG~~

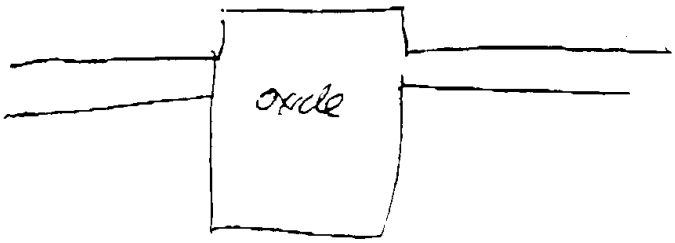
Polish Back to BPSG layer

strip

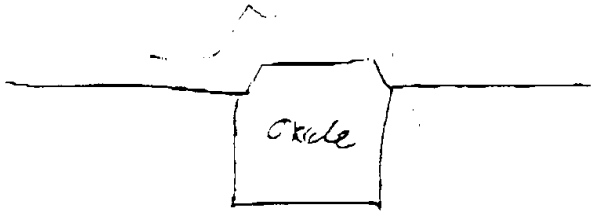


use act strip BPSG ER is N 50 time thermal oxide rate so rough will be

after Strip I



after strip II



Bill Kountz Pete Cotton

S. Hedges

11/15/89

11/17/89

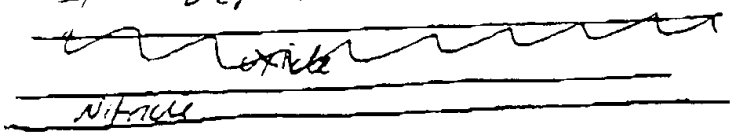
Exhibit B- page 3

STC

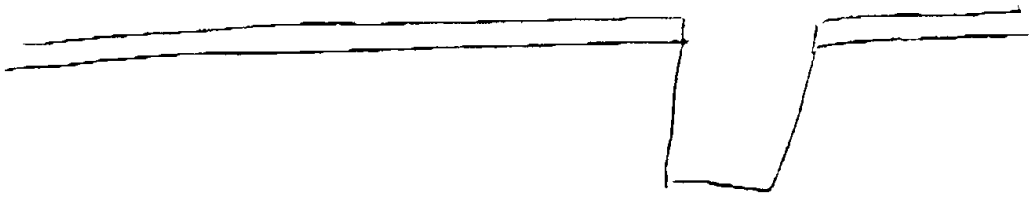
(3) use thin Nitride for STC

Nitride is used only as a means to determin oxide height above Si

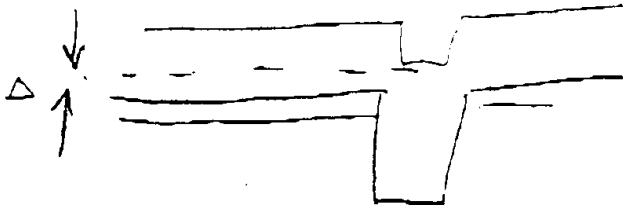
I dep thin Nitride



II mask and etch



III dep HDP oxide or PECVD oxide or APCVD oxide



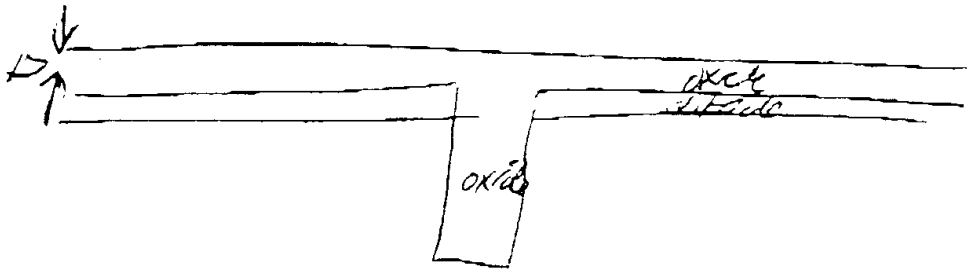
Thickness is targeted to achieve planarity at Δ Å above Si

Bill Kaufmey - Idea
[redacted]
Alan Bloss

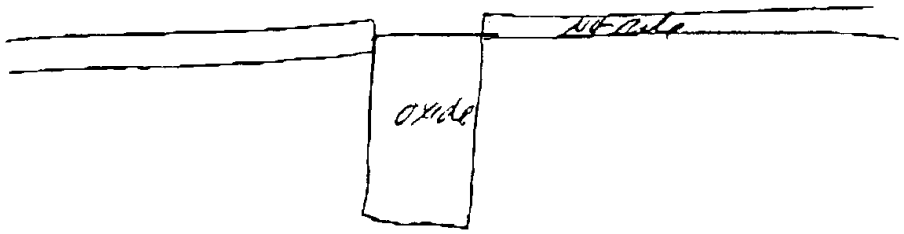
11/15/99
11/15/99

Exhibit B- page 4

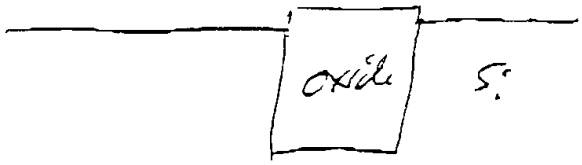
~~IV~~ CMP



V wet strip of oxide



VI nitride strip



Bill Kowsey Kyle Gilboa
S. Hedges
Alan Blum

11/15/99
11/15/99

Exhibit B- page 5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

Serial No.: 09/846,119

Filed: April 30, 2001

For: METHOD OF MAKING A PLANARIZED SEMICONDUCTOR STRUCTURE

Group Art Unit: 1763

Examiner: Goudreau, G.

Atty. Dkt. No.: 5298-04700

CERTIFICATE OF MAILING
37 C.F.R. § 1.18

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

9-19-03
Date

Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, Yitzhak Gilboa, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.

2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

CONCEPTION

3. As supported below, I, along with Steven Hedayati, William W.C. Koutny, Jr. and Krishnaswamy Ramkumar, conceived of the subject matter claimed in the present application within the United States before June of 2000. The subject matter includes a method for forming a structure within a trench of a semiconductor topography.

4. Exhibit A attached hereto is a true copy of an invention disclosure form and attached pages which bear dates before June of 2000 corresponding to the conception of the invention. The actual dates for the first drawings, the first written description and first oral disclosure to others have been redacted.

5. Page 5 of Exhibit A describes the subject matter of the presently claimed case including the use of fixed abrasive polishing techniques to produce structures with a limited amount of dishing.

6. Exhibit B attached hereto is a true copy of a written description of the conceived subject matter, dated before June of 2000.

7. Page 2 of Exhibit B describes the subject matter of the rejected claims including the use of fixed abrasive polishing techniques to polish a layer deposited within a trench.

REDUCTION TO PRACTICE AND DILIGENCE

8. From at least a time just prior to June of 2000 through the filing of the application on April 30, 2001, efforts were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to June of 2000 through the filing of the application on April 30, 2001.

9. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to June of 2000 through the filing of the application on April 30, 2001.

10. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Yitzhak Gilboa

Date: 7/14/03

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S) DISCLOSURE NO PM00028

***

A. Name YITZHAK [illegible] CY Initials [illegible] Empl. No. [illegible] Ext. No. [illegible]

Citizenship U.S.A. Dept # [illegible] Home Phone No. [illegible]

Home Mailing Address [illegible]

***

B. Name William Bintoro CY Initials BK Empl. No 135 Ext. No 3653

Citizenship [illegible] Dept # [illegible] Home Phone No. [illegible]

Home Mailing Address 2555 Homestead #45 Santa Clara, CA 95051
2555 Homestead 45 95051

***

C. Name Steven Hedges CY Initials SSH Empl. No. 9534 Ext. No. 4556

Citizenship U.S. Dept # 3163 Home Phone No. 408-927-9187

Home Mailing Address 124 Valley Quail Circle San Jose CA 95120

2. TITLE OF INVENTION Method of making Sublas trench isolation Structure

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings Redacted
Where can first drawing be found Redacted

B. Date of first written description Redacted
Where is description found Redacted

C. Date of first oral disclosure to others Redacted
To whom? Discussed with KTK SSH BK

4. CONSTRUCTION OF DEVICE

A. Date Completed
B. Was prototype made?
C. By whom made?
D. Where can the prototype be found?

Inventors: [signature] Date 1/24/00

Inventors: [signature] Date 5/24/00

Inventors: [signature] Date 5/24/00

Witnessed, Read, and Understood by: [signature] Date 5/24/00

Witnessed, Read, and Understood by: [signature] Date 5/24/00

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 1

CYPRESS SEMICONDUCTOR

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1. INVENTOR(S) DISCLOSURE NO _____

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A. Name Ramkumar CY Initials KTR Empl. No. 3305 Ext. No. 2720

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Home Mailing Address 1195 LYNBROOK WAY, SAN JOSE, CA 95129

***

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____

Citizenship _____ Dept # _____ Home Phone No. _____

Home Mailing Address _____

***

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____

Citizenship _____ Dept # _____ Home Phone No. _____

Home Mailing Address _____

2. TITLE OF INVENTION _____

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings _____
Where can first drawing be found _____

B. Date of first written description _____
Where is description found _____

C. Date of first oral disclosure to others _____
To whom? _____

4. CONSTRUCTION OF DEVICE

A. Date Completed _____
B. Was prototype made? _____
C. By whom made? _____
D. Where can the prototype be found? _____

Inventors: _____ Date _____

Inventors: _____ Date _____

Inventors: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Each page upon which information is entered should be signed and witnessed

Exhibit A- page 2

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

5. **TEST OF DEVICE**

A. Date: ____ Witness(es): ____

B. Results: ____

6. **SALE**

A. Was invention sold or offered for sale? Yes___ No✓
B. Was invention used to make, assemble or test a commercial product? Yes___ No✓
C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes___ No✓
D. Actual or estimated date of first sale, offer or commercial use ____
E. Is invention part of a product for which there is a data sheet? Yes___ No✓ (If yes, attach a copy)
F. Actual or estimated date of publication, release or availability of data sheet ____

7. **USE**

A. Is invention presently being used? Yes____ No✓

B. In what product or process is invention presently being used?

Are there specific plans for its use in near future? In what products or processes?

RAM-8

8. **RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS**

5,972,792 / 4010535 and 5782675 / 5919282
4393627 / [illegible]

9. **WAS INVENTION** Conceived (Yes____ (No✓ Constructed (Yes____ (No✓ Tested (Yes____ (No✓ during performance of Government Contract?

Contract Number ____
(Give Full Contract Number)

==========

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventor(s): [signature] Date [illegible]
Inventor(s): [signature] Date [illegible]
Inventor(s): [signature] Date [illegible]
Witnessed, Read, and Understood by: [signature] Date [illegible]
Witnessed, Read, and Understood by: [signature] Date [illegible]
Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 3

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
2. Describe old technology, if any, for performing the function of the invention. Provide references, if available.
3. Indicate the disadvantages of the old technology.
4. Describe your invention and its construction, showing the changes, additions and improvements over the old method.
5. Give details of its operation (i.e., how is your invention used?), if not already described under 4.
6. State the advantages of your invention over what has been done before.
7. Indicate any alternate component(s) and/or method(s) of construction.
8. If a joint invention, indicate what contribution was made by each inventor.
9. Describe the features that are believed to be new.
10. State opinion of relative value of invention.

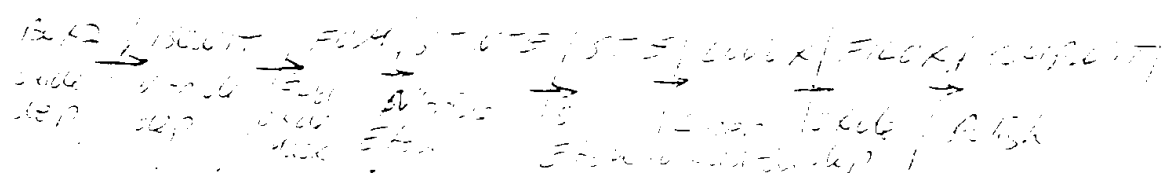
***

11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

==========

1. The purpose of the invention is to improve the manufacturability of STI and reduce cost, i.e. to achieve it by reducing processing steps

2. Current technology (PT-up TDI) calls for the following steps:



Inventors: _____ Date 8/24/00

Inventors: _____ Date 8/24/00

Inventors: _____ Date 8/24/00

Witnessed, Read and Understood by: _____ Date 8/24/00

Witnessed, Read and Understood by: _____ Date 8/24/00

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 4

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

(3.) Disadvantages addressed by invention:

1. Thick mask - layer required to overcome step height in thing caps across the mesa can induce stress defects
2. Additional etch required to etch mask
3. Oxide step edge which step edge could result in poly stringers
4. Thicker oxide film deposition to overcome step edge effect by CMP.

(4) The current invention has three options in using Final, Plastic, poly as the ~~[illegible]~~ material of choice. The main advantage of this process is the negligible amount of residue compared to conventional thing process. The second advantage is self planarization. Option I - no thick hard mask.

In this option no thick mask used. Final is initial on base oxide. Trench etch completes at the stop on oxide. The trench is optimized, the trench etch oxide of [illegible] in the trench and across the thickness of the [illegible] + trench depth variation after [illegible] oxide etch. Fill the oxide for thing. Using Final Mask [illegible] removed [illegible] of oxide. The [illegible] [illegible] [illegible] [illegible] [illegible] [illegible] [illegible] [illegible] [illegible] [illegible]

Inventor(s): [signature] Date [illegible]

Inventor(s): [signature] Date [illegible]

Inventor(s): [signature] Date [illegible]

Witnessed, Read and Understood by: [signature] Date [illegible]

Witnessed, Read and Understood by: [signature] Date [illegible]

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 5

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

Option II - Deposit Thin Nitride -

Grow base oxide grow thin layer of Nitride (0-500Å) expose Field oxide mask, Etch Nitride, Deposit fill oxide polish down to Nitride stop on oxide at a predetermined Residual oxide over the Nitride. Strip Remaining oxide. Strip Remaining Nitride.

Option II

grow base oxide deposit Nitride, expose Field Etch trench, deposit fill oxide, polish to Nitride layer use wet strip to remove remaining oxide, use additional wet strip to remove oxide, Due to wet-etch rate differences of Nitride to oxide etched oxide, strip will result in positive step at Nitride/oxide. Anneal Sacrificial oxide, Strip Nitride, Anneal Sacrificial oxide, Grow Gate oxide, Deposit Poly, Dope Poly, Mask Poly, Etch Poly, Strip Resist, Implant Source/Drain, Anneal, Deposit Oxide, Contact Etch, Deposit Metal, Mask Metal, Etch Metal, Strip Resist, Deposit Passivation, Mask Passivation, Etch Passivation, Strip Resist.

(6) - Same option as (5) except Deposit Nitride instead of oxide. Allowing the use of wet etch to remove Nitride.

(7) - Grow oxide, Deposit Nitride, Mask Nitride, Etch Nitride, Strip Resist, Grow Field oxide, Strip Nitride, Strip Sacrificial oxide, Grow Gate oxide, Deposit Poly, Dope Poly, Mask Poly, Etch Poly, Strip Resist, Implant Source/Drain, Anneal, Deposit Oxide, Contact Etch, Deposit Metal, Mask Metal, Etch Metal, Strip Resist, Deposit Passivation, Mask Passivation, Etch Passivation, Strip Resist.

Inventor(s) _____ Date 8/24/00

Inventor(s) _____ Date 8/24/00

Inventor(s) _____ Date 8/24/00

Witnessed, Read, and Understood by: _____ Date 8/24/00

Witnessed, Read, and Understood by: _____ Date 8/24/00

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 6

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

(8) equal contribution

(9) Fixed abrasive polish, no polish stop, Substrate polish stop

(10) - Invention will enable reduction of cost of ownership compared to Sharp.
- enables STI polish without requirement of Resist mask.
- enables STI polish with reduced step height budget required for .13 um technology.

Inventor(s): _____ Date 6-27-00

Inventor(s): _____ Date 6/27/00

Inventor(s): _____ Date 6-27-00

Witnessed, Read, and Understood by: _____ Date 6/27/00

Witnessed, Read, and Understood by: _____ Date 6/27/00

(Each page upon which information is entered should be signed and witnessed.)

Option 1

- No Nitride HM
- Stop after flatness - fixed abrasive
- Wet dip to below Si

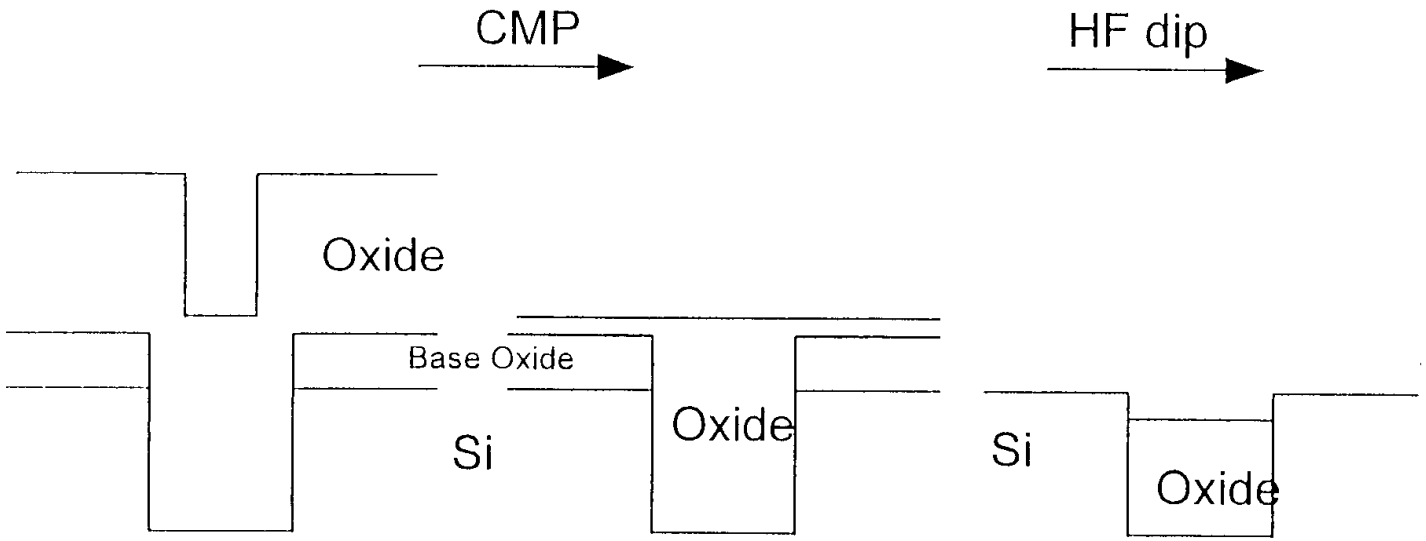
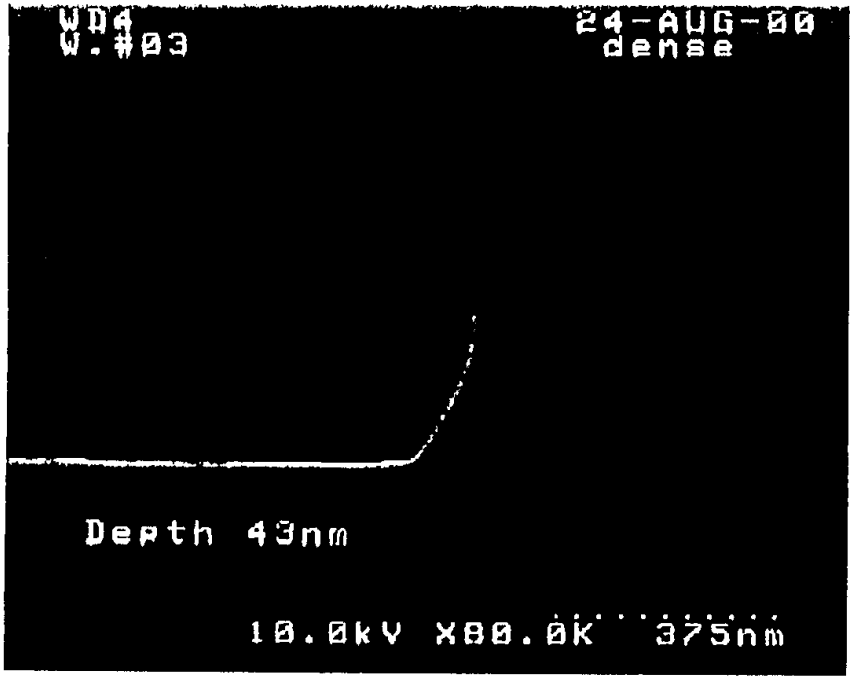


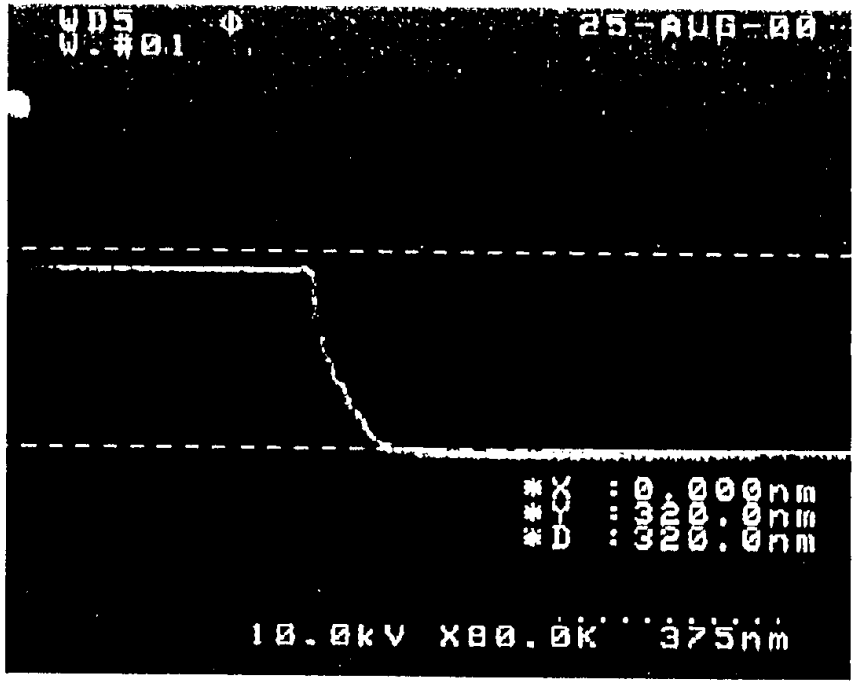
Exhibit A- page 8

Method of Making STI

Exhibit A- page 9

Option 1

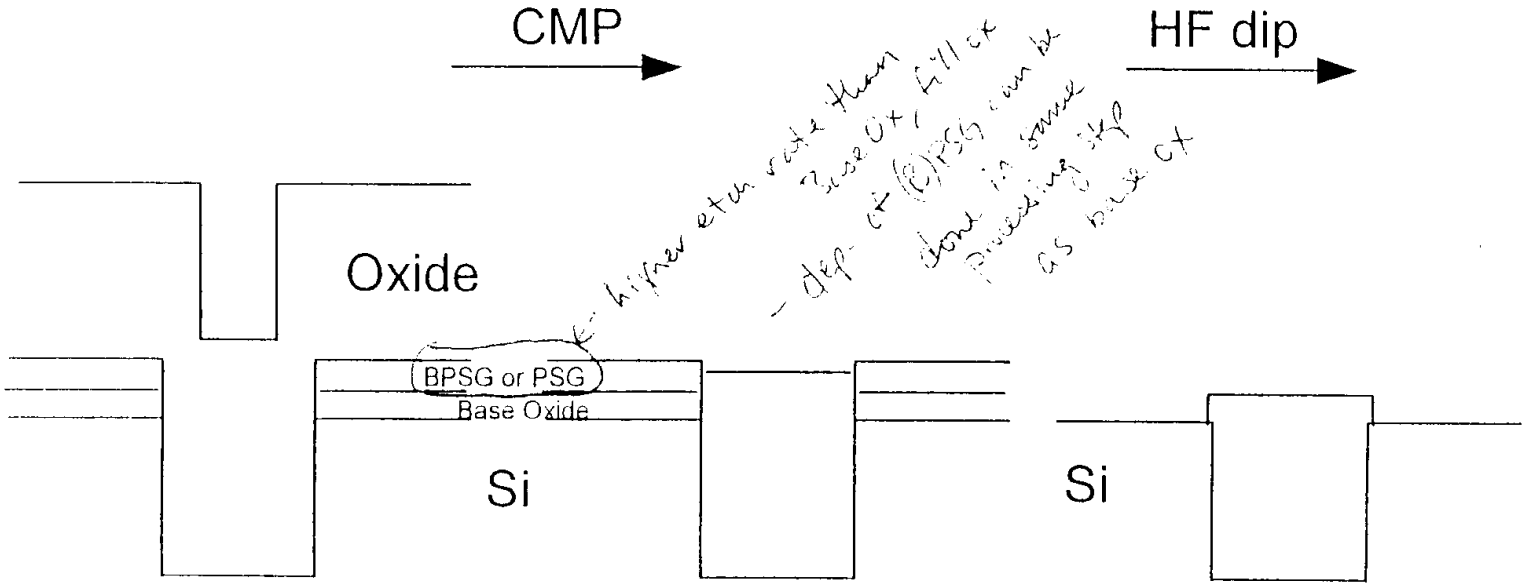




Option 2

Exhibit A - Page 10

- Use doped oxide to increase selectivity during wet Dip
- polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height



Option 3

← old Nit: thick (~2000 Å) to act as CMP polish stop

- Use thin Nitride
- polish to flatness - Fixed Abrasive ,stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step hieght

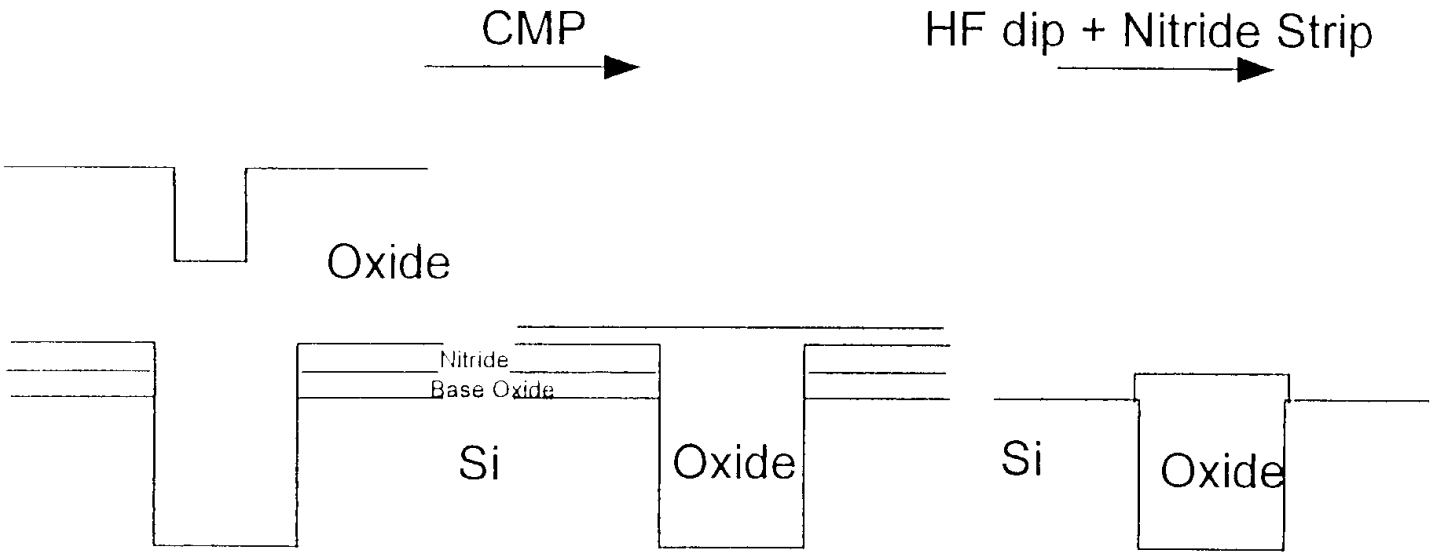


Exhibit A- page 11

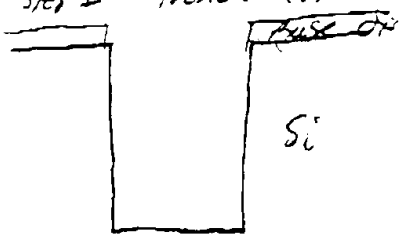
1

STI

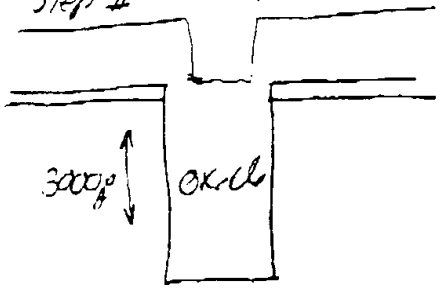
method of making shallow trench isolation structure with no/or thin Nitride CMP Stop.

① No Nitride - using Fixed Abrasive
Proposed by Steven Hedegard 10/15/99.

Step I trench definition



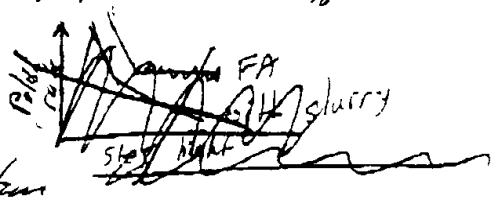
Step II - oxide dep using:
HDP
PECVD
APCVD

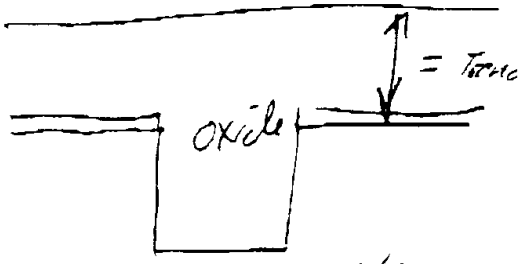


in step II
need to deposit trench depth + trench depth variation

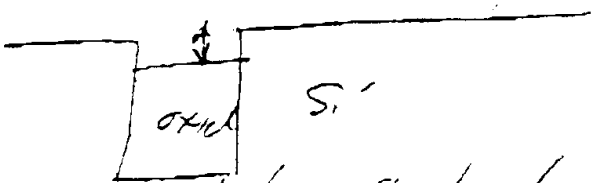
step III Polish

due to Fixed Abrasive properties CMP will self planarize once flatness is achieved.





step IV oxide Strip



Strip will result in oxide below Si level

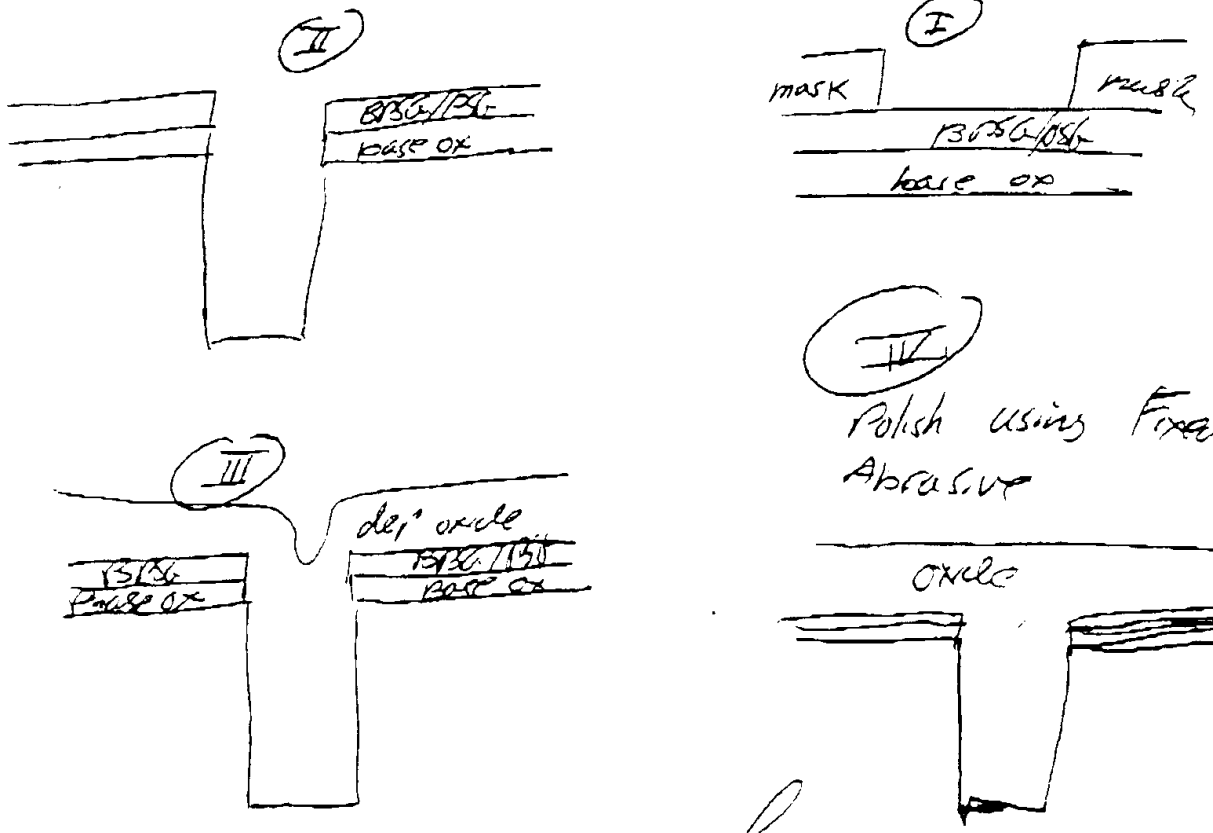
Steven Hedegati, Ramkumar, Bill Keating, Nick Gilbert
S. Hedegati 11/15/99
K. Bhatia 11/15/99

Exhibit B- page 1

STI

as long as Trench depth variation is controlled below a certain number ie ± 500 Å then polish can be done without nitride layer.

(2) 2nd Method use of PSG/BPSG layer as a bas oxide or on top of pad oxide



Bill Routhey

S. Hedges

Alan Block

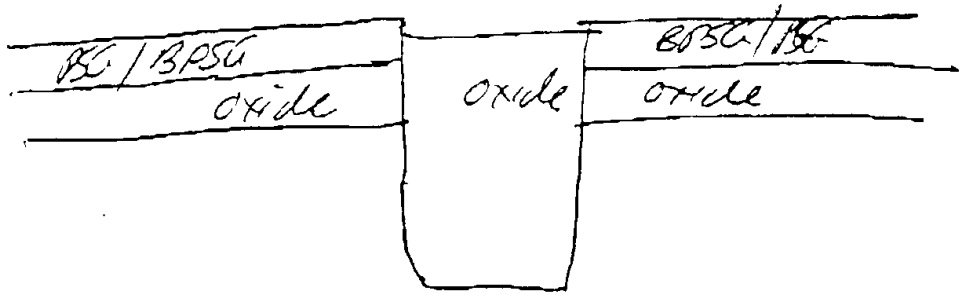
11/15/99

11/15/99

Exhibit B- page 2

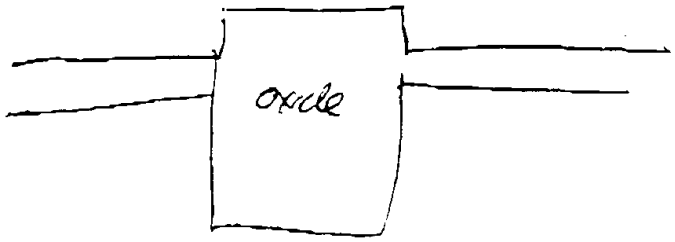
~~Strip Oxide back to BPSG~~

Polish Back to BPSG layer strip

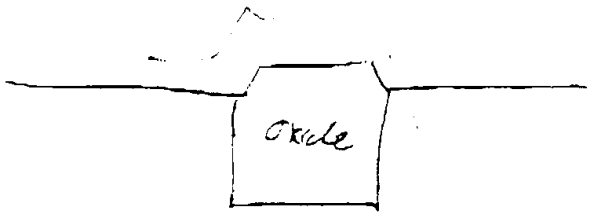


use wet strip BPSG ER is N 50 time thermal oxide rate so reSulk will be

after Strip I



after Strip II



Bill Kountz Nitride Etch

S. Hedges
DA. / ID.

11/15/89
11/15/90

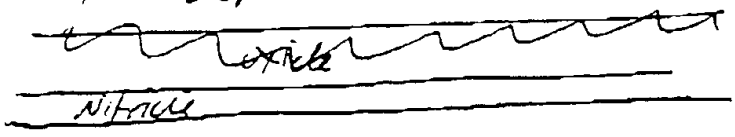
Exhibit B- page 3

STC

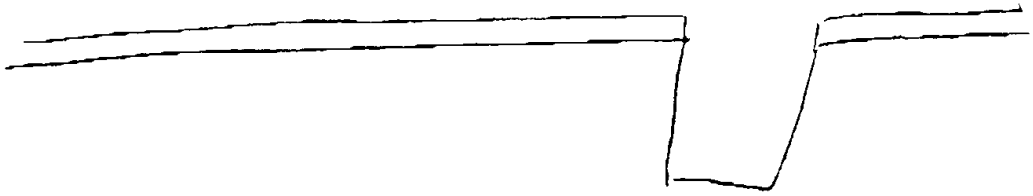
(3) use Thin Nitride for STC

Nitride is used only as a means to determin oxide height above S

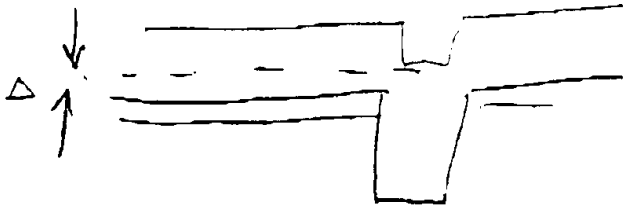
I dep Thin Nitride



II mask and etch



III dep HDP oxide or PECVD oxide or APCVD oxide



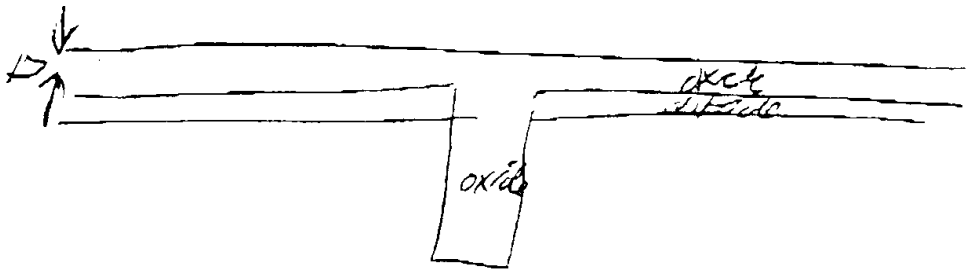
Thickness is targeted to achieve planarity at Δ Å above Si

Bill Kountney - Idea
[redacted]
Alan Bloss

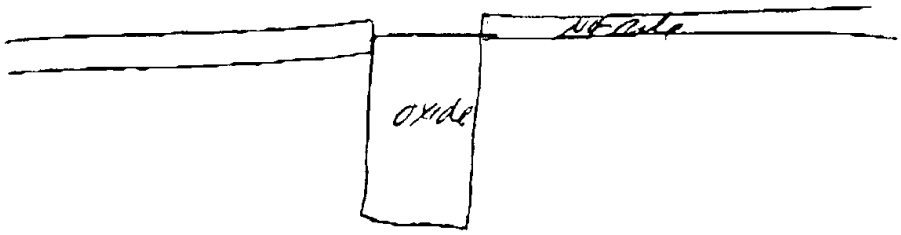
11/15/99
11/15/99

Exhibit B- page 4

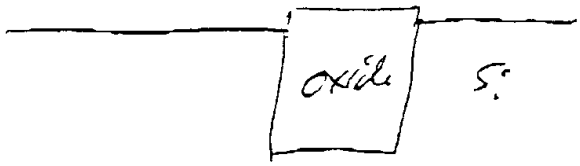
~~IV~~ CMP



V wet strip of oxide



VI nitride strip



Bill Kourtney Kyle Gilbert
S. Hedges
Alan Blum

11/15/99
11/15/99

Exhibit B- page 5